PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION OF THE RECORDING OF A CHANGE

(PCT Rule 92bis.1 and Administrative Instructions, Section 422)

To:

LUZZATTO, Kfir
Luzzatto & Luzzatto
P.O. Box 5352
84152 Beer-Sheva
ISRAËL

Date of mailing (day/month/year)
09 August 2000 (09.08.00)

Applicant's or agent's file reference
4650/WO/98

IMPORTANT NOTIFICATION

International application No.
PCT/IL99/00154

International filing date (day/month/year)
18 March 1999 (18.03.99)

1. The following indications appeared on record concerning:

[X] the applicant [ ] the inventor [ ] the agent [ ] the common representative

Name and Address
SAVAN COMMUNICATIONS LTD.
Hamelacha Street 71a
42504 Netanya
Israel

State of Nationality: IL
State of Residence: IL
Telephone No.:
Facsimile No.:
Teleprinter No.:

2. The International Bureau hereby notifies the applicant that the following change has been recorded concerning:

[X] the person [X] the name [X] the address [ ] the nationality [ ] the residence

Name and Address
INFINEON TECHNOLOGIES AG
St. Martin Strasse 53
D-81541 Munich
Germany

State of Nationality: DE
State of Residence: DE
Telephone No.:
Facsimile No.:
Teleprinter No.:

3. Further observations, if necessary:

4. A copy of this notification has been sent to:

[X] the receiving Office
[ ] the International Searching Authority
[ ] the International Preliminary Examining Authority
[ ] the designated Offices concerned
[X] the elected Offices concerned
[ ] other:

The International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland

Facsimile No.: (41-22) 740.14.35

Authorized officer
I. Britel

Telephone No.: (41-22) 338.83.38

Form PCT/IB/306 (March 1994)

003455962

ATENT COOPERATION TRL TY

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION OF ELECTION

(PCT Rule 61.2)

To:

Assistant Commissioner for Patents
United States Patent and Trademark Office
Box PCT
Washington, D.C.20231
ÉTATS-UNIS D'AMÉRIQUE

in its capacity as elected Office

Date of mailing (day/month/year) 22 December 1999 (22.12.99)	
International application No. PCT/IL99/00154	**Applicant's or agent's file reference** 4650/WO/98
International filing date (day/month/year) 18 March 1999 (18.03.99)	**Priority date** (day/month/year) 19 March 1998 (19.03.98)
Applicant PORAT, Boaz et al	

1. The designated Office is hereby notified of its election made:

[X] in the demand filed with the International Preliminary Examining Authority on:

27 September 1999 (27.09.99)

[ ] in a notice effecting later election filed with the International Bureau on:

2. The election [X] was

[ ] was not

made before the expiration of 19 months from the priority date or, where Rule 32 applies, within the time limit under Rule 32.2(b).

The International Bureau of WIPO **34, chemin des Colombettes** **1211 Geneva 20, Switzerland**	Authorized officer S. Mafla
Facsimile No.: (41-22) 740.14.35	Telephone No.: (41-22) 338.83.38

. ATENT COOPERATION TRL. .TY

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION CONCERNING
AMENDMENTS OF THE CLAIMS

(PCT Rule 62 and
Administrative Instructions, Section 417)

To:

Assistant Commissioner for Patents
United States Patent and Trademark
Office
Box PCT
Washington, D.C.20231
ÉTATS-UNIS D'AMÉRIQUE

in its capacity as International Preliminary Examining Authority

Date of mailing (day/month/year)	
22 December 1999 (22.12.99)	
International application No.	International filing date (day/month/year)
PCT/IL99/00154	18 March 1999 (18.03.99)
Applicant	
SAVAN COMMUNICATIONS LTD. et al	

The International Bureau hereby informs the International Preliminary Examining Authority that no amendments under Article 19 have been received by the International Bureau (Administrative Instructions, Section 417).

The International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland

Facsimile No. (41-22) 740.14.35

Authorized officer

S. Mafla

Telephone No. (41-22) 338.83.38

PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 :
H04B 1/38, 1/50, H04L 5/12, 5/16

A1

(11) International Publication Number: **WO 99/48219**

(43) International Publication Date: 23 September 1999 (23.09.99)

(21) International Application Number: PCT/IL99/00154

(22) International Filing Date: 18 March 1999 (18.03.99)

(30) Priority Data:
123739 19 March 1998 (19.03.98) IL

(71) Applicant *(for all designated States except US)*: SAVAN COMMUNICATIONS LTD. [IL/IL]; Hamelacha Street 71a, 42504 Netanya (IL).

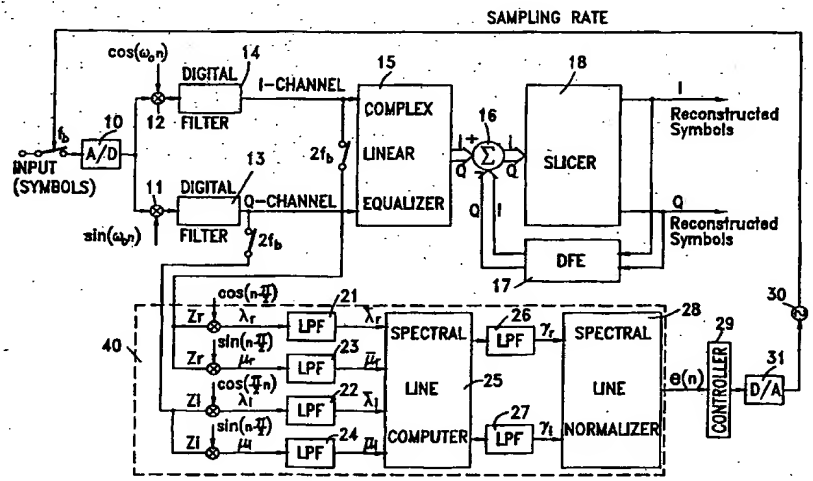
(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: PORAT, Boaz [IL/IL]; Shimshon Street 93, 34678 Haifa (IL). HARPAK, Amnon [IL/IL]; Moshe Dayan Street 62, 58671 Holon (IL). PELEG, Shimon [IL/IL]; Anchilevich Street 11, 45285 Hod–Hasharon (IL).

(74) Agents: LUZZATTO, Kfir et al.; Luzzatto & Luzzatto, P.O. Box 5352, 84152 Beer–Sheva (IL).

(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: METHOD AND APPARATUS FOR CLOCK TIMING RECOVERY IN χDSL, PARTICULARLY VDSL MODEMS



(57) Abstract

Method and modem for fast timing recovery of transmitted data between a master χDSL modem and a slave χDSL modem, over a noisy, high loss, high distortion wiring. Transmitted QAM symbols are received and sampled (10) at the slave modem. The sampled data is split into in–phase (I) and quadrature (Q) channels (11, 12), each of which is filtered by matched filter (13, 14). The filtered I and Q outputs are sampled at twice the symbol rate and the lower and upper band edge components are extracted by modulating each of the sampled sequence of I and Q outputs with two discrete time sequences: $\cos(0.5\pi n) = ...,1,0,-1,0,...$ and $\sin(0.5\pi n) = ...,0,1,0,-1,...$ Each of the resulting products is filtered with a first order low–pass filter (26, 27) and re–sampled again at the symbol rate. The Bit Error Rate is computed (28), and the slave modem switches from blind timing recovery mode, to data directed timing recovery mode, after the Bit Error Rate has sufficiently decreased.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	**ES**	Spain	**LS**	Lesotho	**SI**	Slovenia
AM	Armenia	**FI**	Finland	**LT**	Lithuania	**SK**	Slovakia
AT	Austria	**FR**	France	**LU**	Luxembourg	**SN**	Senegal
AU	Australia	**GA**	Gabon	**LV**	Latvia	**SZ**	Swaziland
AZ	Azerbaijan	**GB**	United Kingdom	**MC**	Monaco	**TD**	Chad
BA	Bosnia and Herzegovina	**GE**	Georgia	**MD**	Republic of Moldova	**TG**	Togo
BB	Barbados	**GH**	Ghana	**MG**	Madagascar	**TJ**	Tajikistan
BE	Belgium	**GN**	Guinea	**MK**	The former Yugoslav Republic of Macedonia	**TM**	Turkmenistan
BF	Burkina Faso	**GR**	Greece			**TR**	Turkey
BG	Bulgaria	**HU**	Hungary	**ML**	Mali	**TT**	Trinidad and Tobago
BJ	Benin	**IE**	Ireland	**MN**	Mongolia	**UA**	Ukraine
BR	Brazil	**IL**	Israel	**MR**	Mauritania	**UG**	Uganda
BY	Belarus	**IS**	Iceland	**MW**	Malawi	**US**	United States of America
CA	Canada	**IT**	Italy	**MX**	Mexico	**UZ**	Uzbekistan
CF	Central African Republic	**JP**	Japan	**NE**	Niger	**VN**	Viet Nam
CG	Congo	**KE**	Kenya	**NL**	Netherlands	**YU**	Yugoslavia
CH	Switzerland	**KG**	Kyrgyzstan	**NO**	Norway	**ZW**	Zimbabwe
CI	Côte d'Ivoire	**KP**	Democratic People's Republic of Korea	**NZ**	New Zealand		
CM	Cameroon			**PL**	Poland		
CN	China	**KR**	Republic of Korea	**PT**	Portugal		
CU	Cuba	**KZ**	Kazakstan	**RO**	Romania		
CZ	Czech Republic	**LC**	Saint Lucia	**RU**	Russian Federation		
DE	Germany	**LI**	Liechtenstein	**SD**	Sudan		
DK	Denmark	**LK**	Sri Lanka	**SE**	Sweden		
EE	Estonia	**LR**	Liberia	**SG**	Singapore		

METHOD AND APPARATUS FOR CLOCK TIMING RECOVERY IN XDSL, PARTICULARLY VDSL MODEMS

Field of the Invention

The present invention relates to digital data communication between two locations over the connecting wiring. More particularly, the invention relates to the use of Very High speed Digital Subscriber Loop (VDSL) modems for transferring data at high rates between two locations connected at least partially by conventional, twisted copper wires.

Background of the Invention

The art has devoted considerable attention to the problem of transmitting data in a high rate between users being at different locations. Such users, may be home Personal Computers (PCs), office desktop workstations, cable television broadcasting services, Local Area Networks (LANs) and others. In some applications users are connected to each other by modems (modulator-demodulator) which encode the digital data to be delivered from one point (user) to another point and transmit the encoded data through a data link which may be, for instance, an analog communication channel. Such data comprises voice, digital video movies and software data files.

Digital Subscriber Loops (DSLs) comprise several technologies for high data rates, e.g., Asymmetric Digital Subscriber Loops (ADSLs), High speed Digital Subscriber Loops (HDSLs) and Very High speed Digital Subscriber Loops (VDSLs). Generally, the whole family of DSLs is commonly known as XDSL. In some VDSL applications, like video

transmission, data should be transmitted in very fast rates, usually up to 12.96 Mb/Sec or even exceed 25.92 Mb/Sec.

Analog modems were developed to deal with data rates up to 33.6 Kb/Sec. This rate is unacceptable for many applications, e.g., picture transmission where pictures are constructed from large data files. Digital modems which are developed to work on leased copper lines between two locations can reach higher data rates, up to 64 Kb/s or even 128 Kb/s. However, this rate is still too low for many applications. Any transmission medium interferes with the transmitted data by adding noise, by attenuating its amplitude, and by changing its phase. Digital modems suffer from these phenomena, reducing their ability to receive data without errors. Errors are critical in digital modems.

LANs are very intensively used to connect users, usually in the range of a single building but in many cases the range is expanded to several buildings. Since in many cases it is desired to connect users being in different buildings to share same data base, it is generally desired to exploit for this purpose an existing PSTN twisted pair line, or preferably a leased line. Moreover, in many cases it is desired to make high rate data communication between two LANs, for example, LANs of two offices located in different cities a hundred miles or more away from one another.

There are known connections that can provide higher bandwidth than twisted pair copper lines, for example, 10/100-Base-T coaxial cables and fiber-optic lines. The copper lines between PABXs were already replaced by fiber-optic lines in most cases,

and have become standard. However, it is not foreseen that in the near future the twisted pair copper lines between the telephone end users and the PABXs be replaced, due to their huge number, and to the complexity of replacing them. Therefore, it is desirable to provide a much higher rate modem communication on the relatively narrow bandwidth twisted pair copper lines. Significant efforts are now put in order to develop higher rate modems, which are commonly called in the art, VDSL modems.

Basically, the conventional unshielded copper wire twisted pair was originally designed to provide a medium for voice transmission, and when it is used in telephone communication its bandwidth is confined by filters in its two ends to between 300 Hz to 3.4 KHz. In leased lines, a wider bandwidth is available, however the possible data rate is still limited by the fact that long lines introduce very large attenuation, especially in the higher range of the bandwidth, which exceeds 8 MHz in VDSL modem transmission. This relatively wide bandwidth is required to enable full duplex communication channel, utilizing the known Frequency Division Duplex (FDD). Moreover, telephone lines pass through switching exchanges conducted by the local telephone companies, and this may be a very noisy environment which disrupts the transmitted data.

Usually, digital $\mathcal{X}$DSL modems utilize Quadrature Amplitude Modulation (QAM) techniques to encode data. In this technique, the transmitted information-carrying signal appears in pre-defined amplitude and phase states, each state representing a pre-determined number of bits, and is termed "a symbol". Conventional QAM techniques utilize 16 states (symbols) or 64 states. In case of 64-QAM, each symbol represents 6

bits. Therefore, for a desirable VDSL modem transmitting at a rate of 12.96 Mb/Sec, $2.16*10^6$ symbols have to be transmitted in each second. A one kilometer twisted pair line has a propagation delay (impulse response time) in the range of about 12 μSec, whereas each symbol duration is 0.463 μSec in the above case. Thus, the effective duration of the line impulse response is about 25 symbols. This long duration of the impulse response of the line leads to a severe Inter symbol Interference (ISI) which may result in a large errors at the receiving modem if cannot canceled, and practically limits the data rate.

The communication between two $\mathcal{X}$DSL modems is carried out while one modem is the transmitter (master) and the other is the receiver (slave). Data directed to the slave modem are termed "downstream" while the data directed to the master modem are termed "upstream". Communication between the two modems requires synchronization between their timing clocks. Proper operation of $\mathcal{X}$DSL systems requires almost perfect synchronization between master and slave clocks, which means that they must work at the same frequency. Any constant frequency offset leads to a constant growing phase error which may lead to mismatch between the number of transmitted and received symbols per time unit, which is unacceptable. Different clocks always have somewhat different frequencies due to manufacturing tolerances, aging (changes in their component characteristics versus time), temperature variations, power supply tolerances, random noise deviations, etc. Therefore, synchronization means are required in the slave modem to recover the master clock frequency (timing) from the transmitted symbols, together with a correction apparatus to lock the slave clock frequency to the master clock frequency.

One known method for synchronization between receiving and transmitting modem clocks is performed by the transmission of a pilot tone from the master modem to the slave modem. However, in case of pilot tone transmission the energy is concentrated in a single frequency, violating the Power Spectral Density (PSD) constraints and interfering with other systems operating in the same frequency range. It is generally desirable that the power of the synchronizing signal will be distributed on a wide frequency band, but usually these signals are not periodic. Therefore, using distributed power signals for synchronization of $\mathcal{X}$DSL systems is problematic.

Considering the aforementioned problems, an $\mathcal{X}$DSL system is required to synchronize in "blind" mode, which means operating in a very noisy environment when initially there is no information about the transmitted symbols at the receiving modem. This mechanism is known as Blind Timing Recovery (BTR). It is characterized by the fact that all symbols have equal probabilities and some or most of them are attenuated, resulting in a very bad Signal to Noise Ratio (SNR) and/or being received with a random phase-shift and with high additive noise. BTR algorithms face significant difficulties when trying to reconstruct the master clock. Thus, an effective error correction mechanism is required, without reducing the data rates.

Several suggested solutions for BTR have been proposed. "Passband Timing Recovery in an All-Digital modem receiver" by D. Godard, IEEE Transactions on Communications, Vol. COM-26, No. 5, 1978, p.p. 517-523, the disclosure of which is incorporated herein by reference describes a method of performing BTR. However, this

reference does not provide a mathematical proof, or show any means for carrying it out.

An effort to carry out Godard's method is discussed in "Joint Blind Equalization, Carrier Recovery, and Timing Recovery for High Order QAM Signal Constellation", IEEE Transactions on Signal Processing, Vol. 40, No. 6, 1992, p.p. 1383-1398 the disclosure of which is also incorporated herein by reference. This reference describes means for performing BTR by applying a complicated algorithm, based on Godard's theory. Particularly, these means require complicated hardware having extremely high processing power.

It is an object of the present invention to provide a synchronization method useful for fast bi-directional data transmission , between xDSL modems over conventional unshielded copper or the like wiring, for example connecting LANs.

It is another object of the present invention to provide a simple fast method for accurately recovering the clock frequency of the transmitting xDSL modem at the receiving modem, without the need of a predetermined training sequence.

It is a further object of the invention to provide a method for fast synchronization of the receiving xDSL modem clock to the transmitting xDSL modem clock, while operating in blind mode

It is still another object of the invention to provide adaptive, fast converging error correction apparatus for carrying out the method of the invention.

Other objects and advantages of the invention will become apparent as the description proceeds.

SUMMARY OF THE INVENTION

The invention is directed to a method for fast timing recovery of transmitted data between two xDSL modems, said data is transferred trough a noisy, high loss, high distortion wiring, comprising the steps of:

a) Providing a master xDSL modem, synchronized by its own timing clock, for data transmission to a second slave xDSL modem;

b) Providing a second slave xDSL modem, synchronized by its own timing clock, for data reception from said master xDSL modem;

c) Providing a communication wiring connecting said master modem to said slave modem;

d) Encoding and transmitting the desired data as a sequence of symbols to the slave modem using pre-determined QAM states;

e) Receiving the transmitted symbols at the slave receiver (demodulator);

f) Sampling the received signal;

g) Splitting the sampled data to in-phase (I) and quadrature (Q) channels;

h) Filtering each channels of step g) above with digital low-pass filters, said filters being matched to the transmitting filters at the master modem;

i) Turning the master clock timing recovery into blind mode, by the steps of:

(1) Sampling the filtered I and Q outputs at twice the symbol rate;

(2) Extracting the lower and upper band edge components by modulating each of

the sampled sequence of I and Q outputs of step (1) above with two discrete time sequences: $\begin{matrix}\cos(0.5\pi n)=\ldots,1,0,-1,0,\ldots \\ \sin(0.5\pi n)=\ldots,0,1,0,-1,\ldots\end{matrix}$;

(3) Filtering the four resulting products with four first order low-pass filters and re-sampling the results at the symbol rate;

(4) Computing the real and imaginary parts of the spectral line vector using the products of step (3) above;

(5) Filtering both the real and the imaginary parts of step (4) above, using another first order low-pass filter;

(6) Normalizing the magnitude of the spectral line vector to unity using a suitable automatic gain control circuitry;

(7) Extracting the phase of the spectral line vector from the normalized imaginary part of step (6) above;

(8) Feeding the sampled imaginary part of step (7) above as a phase-error signal to a controller of a phase-locked loop (PLL), said PLL utilizing a frequency controlled clock oscillator, the frequency of which is tuned to track the frequency of the incoming symbols (the master modem clock frequency);

(9) Converting the digital control word to analog control voltage supplied to the tracking oscillator of step (8) above, using a Digital to Analog Converter (DAC); and

(10) Using a secondary accumulator to correct the control word supplied to the DAC of step (9) above;

j) Feeding the I and Q filtered outputs to a complex linear equalizer for coarse phase and amplitude error correction;

k) Computing the symbol state data decisions using a slicer circuitry;

l) Fine equalization of the channel distortions by feeding the I and Q outputs of the slicer to a decision feedback equalizer, the outputs of which are extracted from the slicer I and Q inputs, respectively;

m) Computing the extracted symbols error rate at the slicer outputs; and

n) After the error probability decreases to a given Bit Error Rate (BER), switching from blind mode timing recovery to data directed timing recovery mode.

According to a preferred embodiment of the invention the transmission medium is a pair of copper wires, which may be a telephone line. High data rates may be transmitted on relatively long conventional telephone lines, occupying corresponding frequency bands. The timing oscillator of the receiving modem may be a Voltage-Controlled Crystal Oscillator (VCXO), utilized by a phase-locked loop.

According to a preferred embodiment of the invention, blind timing recovery is achieved using a reduced constellation that includes only equal amplitude symbols. This reduced constellation simplifies and accelerates the equalizing process. Error correction process is performed to control the frequency of the PLL tracking oscillator. The error signal produces a digital correction signal which is converted to an analog control signal by a simple Digital to Analog Converter (DAC). Additional secondary accumulator circuitry is utilized to correct the input word to the DAC to attenuate frequency jitter, comprising the steps of:

a) Rounding the double precision control signal;

b) Generating an error signal between the double precision value and the rounded value;

c) Accumulating the error signal in a secondary accumulator;

d) Adding the error signal to the output signal of the secondary accumulator;

e) Comparing the result of step d) above with half the value of the DAC's Least Significant Bit (LSB);

f) Compensating the rounded value according to the result of step e) above by the steps of:

(1) Adding the value of the DAC's LSB to the accumulator output, if the output value is larger than half the value of the DAC's LSB; or

(2) Subtracting the value of the DAC's LSB from the accumulator output, if the output value is smaller than half the value of the DAC's LSB;

Using this a simple DAC together with the digital compensation circuitry simplifies and reduces the cost of the control circuitry, and still maintains a stable, accurate control voltage to the VCXO.

Brief Description of the Figures

The above and other characteristics and advantages of the invention will be better understood through the following detailed description of preferred embodiments thereof, with reference to the appended figures, wherein:

Fig. 1 schematically illustrates a full duplex data communication channel between master and slave xDSL modems;

Fig. 2A is a graph of typical frequency bands occupied by VDSL transmission;

Fig. 2B is a graph of the attenuation of a typical copper wire communication line;

Fig. 3 is a graph of the Impulse-Response (IR) of the communication line of Fig. 2B;

- Fig. 4 illustrates a 16 QAM generation and the resulting 16 state constellation;
- Fig. 5A is a block diagram of the demodulator of the slave modem;
- Fig. 5B is a block diagram of a first order low-pass filter of Fig. 5A;
- Fig. 6 schematically illustrates the output decisions of the slicer of Fig. 5A;
- Fig. 7 is a block diagram of the controller of Fig. 5A; and

Fig. 8 schematically illustrates the phase shift of a 16 QAM constellation resulting from frequency mismatch between master and slave modems clock.

Detailed Description of Preferred Embodiments

Fig. 1 illustrates a full duplex data communication channel between master and slave xDSL modems, using standard telephone line made from copper wires pair. A timing clock 4, which may be supplied by the local telephone system or by a Synchronous Digital Hierarchy (SDH) system, drives the master modem to transmit data (symbols) downstream to the slave modem 2. The slave modem is driven by another clock 5, which is a part of the slave's demodulator 3. Clock 5 should be synchronized to clock 4 since the clock defines the difference between symbols. After synchronization, clock 5 times the downstream symbol reception and upstream symbol transmission to the master modem.

The frequency spectrum of an $\mathcal{X}$DSL channel utilizes two separated frequency bands using Frequency Division Duplex (FDD) as shown in Fig. 2A. The first band 6 occupies the range from 0.9 MHz to 3.5 MHz and is used for down-stream transmission, whereas the second band 7, occupies the range from 4 to 7.9 MHz and is used for up-stream transmission. A 500 KHz Guard-Band (GB) 8 remains unused (by $\mathcal{X}$DSL systems) due to amateur radio interference constraints.

Fig. 2B shows the attenuation of typical copper lines for common diameters (0.35, 0.4, 0.5, and 0.6 mm). From the figure, it can be seen that a typical, 100 m long, telephone line with 0.4 mm copper wire diameter has large attenuation characteristics with sharp attenuation from low to high frequencies. Thus, transmitted symbols propagating along a 1 Km long line reach the slave modems with power attenuation of up to 50 dB. Moreover the line causes a substantial shift of the symbols phase. In addition, since the line passes through switching junctions and other telephone service paths, a lot of noise and cross-talk are added to the attenuated symbols. All these factors distort the amplitude and phase characteristics of the transmitted symbols, making the task of their timing recovery very complicated.

The attenuation of the line is smaller at the downstream band. Therefore, the BTR process at the slave modem can work with a better SNR than by working on the upstream data. By the SNR consideration, downstream data is encoded with 64-state QAM whereas upstream data is encoded with only 16-state QAM. Basically, 16 QAM has better noise immunity than 64 QAM, but wider bandwidth.

Fig. 3 is a graph of the Impulse-Response (IR) of a 1 Km long line. The IR of a system represents the output of the system when applying a unit sample $\delta(n)$ at the input. It is seen that the IR lasts a time period equal to the duration of 25 symbols. Thus, large errors may occur at the slave modem. In addition, fast data rates require extremely fast processing speeds, which limits the complexity of the BTR that may be used.

Fig. 4 illustrates a 16 QAM generation and the resulting state constellation. Two carriers $V*\cos(\omega_0 t)$ and $V*\sin(\omega_0 t)$, shifted by 90°, forming an In-phase channel (I-channel) and Quadrature channel (Q-channel) respectively, are modulated by two information signals S_I and S_Q respectively. Each signal S_I or S_Q assume four values: ±1 and ±3. I and Q channels are summed forming a 16 state QAM signal. These 16 states are distinguishable by their amplitude/phase combinations as illustrated in the constellation diagram in the complex plain. Each state is a vector (symbol) which is the sum of two vectors, I and Q. Since each of S_I and S_Q have four different amplitudes, each may represent four different logic combinations (00, 01, 10, 11). Thus, summations of their respective modulated carriers provide 16 different vectors (symbols), representing 16 logic combinations (0000, 0001, 0010,.....,1111).

Fig. 5A is a block diagram of the demodulator of the slave modem. Symbols are sampled and converted to a digital form by an Analog to Digital (A/D) converter 10. The samples are fed into two multipliers 11 and 12, which are phase-shifted by 90°, forming the I and Q channels. These I and Q channels are filtered by Low Pass Filters (LPF) 13 and 14, respectively. These filters (commonly known as "Nyquist Filters") are

identical, and similar filters exist in the master modem to give it a raised cosine shape. An excess bandwidth of approximately 20% results in these filters.

The filtered I and Q channels are fed into a complex Linear Equalizer (LEQ) 5, which functions as an adaptive filter for a coarse error correction mechanism. LEQ 5 is able to correct both amplitude and phase errors caused by the line. LEQ 5 feeds both I and Q corrections to a slicer 18, which provides a decision for any received symbol in order to classify each symbol to one of the ideal QAM states. The outputs from the slicer 18 are reconstructed symbols, which are fed back into the complex Decision Feedback Equalizer (DFE) 17, via the adder 16, into the slicer 18. The DFE provides an additional fine error correction mechanism which is adaptive according to the resulting errors from the slicer.

Fig. 6 illustrates the output of the slicer 18. The slicer 18 slices the I-Q complex plain to 16 identical squares. For each equalized (by LEQ 15) symbol that falls into one of these squares, a decision is taken to associate it to one of the states. In practice, each received symbol appears with an error in its amplitude as well as in its phase. As a result, all symbols that are associated with a state form a "cluster" around their state. Each DFE reads the errors (distance from the theoretical state) of each symbol, processing the information to predict a better correction step and feeds an input back to the slicer to reduce the error at the next symbol.

Looking back at Fig. 5A, a Timing Recovery Loop (TRL) 40 samples the information of both I and Q channels filtered by LPF 13 and 14 respectively, and provides an error

signal e(n) which is fed to controller 29. The controller accepts the error signal and provides a correcting control voltage (in a direction that reduces the error signal) to a Voltage Controlled Crystal Oscillator (VCXO) 30 that determines the sampling rate of the incoming symbols. This sampling rate should follow the incoming symbol rate (synchronization) and therefore, the TRL 40 together with controller 29 and VCXO 30 are essentially a Phase-Locked Loop (PLL).

TRL 40 may function in two possible modes. The first mode is a blind mode which operates first, until the symbol error rate at the output of the slicer 18 is better than 10^{-3} or any other desired error-rate. After the desired error rate is obtained, the TRL switches to Decision Directed Timing Recovery (DDTR) mode, which is relatively simple and widely used in modems.

Generally, PLLs operate as Frequency Modulation (FM) demodulators. In this case, the frequency of the VCXO should follow the frequency of the master modem clock (incoming symbol rate). A PLL is used to lock the frequency of the timing clock of the slave to that of the master. Any change in the master clock frequency (FM), causes TRL 40 to generate an error signal and the controller reacts by forcing the control voltage of the VCXO to change its frequency to the new frequency. Thus, the VCXO control voltage detects the frequency changes of the master modem clock.

For a simpler and easier understanding of loop operation, a mathematical representation of the VCXO operation is provided below. The VCXO, which is the plant of the control loop, can be mathematically represented as an integrator, because its phase is

proportional to the integral of the frequency and the control voltage of the VCXO determines the instantaneous frequency. Mathematically:

$$v_{vcxo}(t) = \sin[2\pi K_{vcxo} \int c(t)dt] \qquad \textbf{[Eq. 1]}$$

where c(t) is the VCXO control voltage, $v_{vcxo}(t)$ is the VCXO output voltage, and K_{vcxo} is a proportionality constant.

The critical parameter of the VCXO is its instantaneous phase, which is given by:

$$\phi(t) = 2\pi K_{vcxo} \int c(t)dt \qquad \textbf{[Eq. 2]}$$

If $\phi_{in}(t)$ denotes the phase of the incoming signal, then the output of the TRL 40 (which functions as an error signal generator) is given by:

$$e(t) = \sin[\phi_{in}(t) - \phi(t)] \qquad \textbf{[Eq. 3]}$$

Here, the phase error is small and the approximation $\sin x \approx x$ may be used. Hence, the phase error is given by $e(t) \approx \phi_{in}(t) - \phi(t)$ and both the VCXO 30 and the error signal generator are considered as Linear Time Invariant (LTI) systems. Therefore, the controller 29 may also be LTI.

The mathematical description of the above and of the following functions of the loop utilizes both continuous and discrete time analysis, for the sake of convenience. Since digital processing techniques are implemented, a sampling time interval T_0 of the incoming signals is defined, enables normalizing frequencies to the sampling frequency $1/T_0$ and expressing phase in terms of periods. Using the well known Laplace Transform (LT) for transforming time presentation of signals to s domain presentation ($s = \sigma + j\omega$,

where $j^2 = -1$), the transfer function of the VCXO is given by:

$$G(s) = \frac{2\pi K_{vcxo}}{s}. \qquad \textbf{[Eq. 4]}$$

Fig. 7 is a block diagram of the controller, comprising two functional blocks: an LPF 50, which attenuates the additive noise of the error signal e(t) and a proportional/integral controller 51, which provides a correction voltage proportional to the frequency offset between the VCXO and the master modem clock, reducing the steady state phase error to zero. In addition, an integrative controller smoothes the transition of the TRL from blind mode to DDTR mode. The expression of the controller transfer function in the s domain is given by:

$$H(s) = \frac{\omega_0}{2\pi K_{vcxo}} \cdot \frac{s + (\omega_0 / r)}{s} \cdot \frac{1}{1 + (s / \omega_0 r)}. \qquad \textbf{[Eq. 5]}$$

where ω_0 is the loop cutoff frequency (the maximum frequency error that the loop is able to track) and r is the loop damping factor (an indication of the loop reaction and stability). The first expression of H(s) stands for constant gain, the second for proportional/integral part of the controller, and the last one stands for LPF. At the cutoff frequency ω_0, the magnitude of the open loop transfer function is given by (for $s = j\omega_0$):

$$| G(j\omega_0)\, H(j\omega_0) | = 1 \qquad \textbf{[Eq. 6]}$$

The denominator (known as the characteristic polynomial) of the loop transfer function G(s) H(s) is given by:

$$P(s) = s^3 + \omega_0 r s^2 + \omega_0^2 r s + \omega_0^3. \qquad \textbf{[Eq. 7]}$$

this cubic polynomial has one real root and two complex conjugate roots, which determine the damping factor r of the loop. For $r < 1$ the loop is unstable (oscillatory)

and for $r \geq 3$ the loop is overdamped.

According to another preferred embodiment of the present invention, r is chosen to be $r = 2.8$. Since the loop is a PLL, there is a maximum frequency offset Δf_{max} between the master modem clock and the VCXO for which the loop can achieve locking. According to a preferred embodiment of the present invention, ω_0 is chosen to satisfy the condition $\omega_0 \geq 2\pi\Delta f_{max}$ to enable locking.

Rearranging the expression for H(s) a product of two factors gives:

$H(s) = H_1(s)\, H_2(s)$, or

$$H(s) := \frac{1}{1 + \frac{s}{\omega_0 \cdot r}} \cdot \left(K_1 + \frac{K_2}{s} \right) \qquad \textbf{[Eq. 8]}$$

where

$$K_1 := \frac{\omega_0}{2 \cdot \pi \cdot K_{vcxo}} \qquad \textbf{[Eq. 9]}$$

$$K_2 := K_1 \cdot \frac{\omega_0}{r} \qquad \textbf{[Eq. 10]}$$

According to a preferred embodiment of the present invention, K_{vco} is chosen to be $K_{vco} = \Delta f_{max}$. This means that a unity control signal supplied to the VCXO is able to shift its frequency by Δf_{max}.

According another preferred embodiment of the present invention, ω_0 is chosen to be:

$$\omega_0 = 2\pi\beta\Delta f_{\max} \qquad \textbf{[Eq. 11]}$$

where $1 \le \beta \le 2$. Hence, under the above selected conditions K_1 and K_2 are given by:

$$K_1 = \beta \qquad \textbf{[Eq. 12]}$$

$$K_2 = \frac{2\pi\beta\Delta f_{\max}}{r} \qquad \textbf{[Eq. 13]}$$

After the analysis of the controller has been done in s domain, a digital implementation of the LPF $H_1(s)$ and the proportional/integrative controller $H_2(s)$ is done using the well known Z transform. Applying the Z transform on the LPF transfer function $H_1(s)$, the expression in z domain is given by:

$$H_1(z) = \frac{a}{1-(1-a)z^{-1}}, \quad \text{where } a = \omega_0 r. \qquad \textbf{[Eq. 14]}$$

The above expression is a good approximation to perfect discretization of $H_1(z)$, since the loop bandwidth is very small compared with the symbol rate. Thus , $\omega_0 r \ll 1$ and the difference equation related to $H_1(z)$ is given by:

$u[k] = u[k-1] + a \cdot (e[k]-u[k-1])$ where e[k] and u[k] are the input and output signals of the LPF, respectively. Since a is very small, the output u[k] is accumulated in double precision.

Applying the Z transform on the proportional/integral controller transfer function $H_2(s)$, the expression in z domain is given by:

$$H_2(z) = K_1 + \frac{K_2}{1-z^{-1}}. \qquad \textbf{[Eq. 15]}$$

The difference equation related to $H_2(z)$ is given by:

$$y[k] = y[k-1] + (K_2/K_1)\,u[k] \qquad \textbf{[Eq. 16]}$$

$$c[k] = (K_1)\,(u[k]+y[k]) \qquad \textbf{[Eq. 17]}$$

where u[k] is the output signal from the LPF, y[k] is the state variable of the proportional/integral controller, and c[k] is the output of the controller (control signal to the VCXO). In this case $K_1 = 1$ and since K_2 is very small, the output y[k] is accumulated in double precision.

According to a preferred embodiment of the present invention, an 8 bit Digital to Analog Converter (DAC) 31, is used to generate the control signal for the VCXO, for an accurate, simple, cost-effective implementation. This requires rounding of c[k] to be a relatively short number, which results in an unacceptable operation of the loop. The problem is overcome by a method based on the addition of a dither to the control signal c[k], the duty-cycle of which is determined by the rounding error, comprising the following steps:

1) Defining an error $\tilde{c}[k] = c[k] - \hat{c}[k]$ between the double precision value $c[k]$ and its rounded value $\hat{c}[k]$.

2) Adding the error $\tilde{c}[k]$ to a secondary accumulator (integrator) with output $x[k]$. Hence, its output is given by:

$$x[k] = x[k-1] + \tilde{c}[k]. \qquad \textbf{[Eq. 18]}$$

3) Correcting the rounded value of $\hat{c}[k]$ according to the value of $x[k]$. If the Least Significant Bit (LSB) of the DAC is b, the correction is given by:

$$\begin{aligned} x[k] > 0.5b &\Rightarrow \hat{c}[k] = \hat{c}[k] + b,\ x[k] = x[k] - b, \\ x[k] < -0.5b &\Rightarrow \hat{c}[k] = \hat{c}[k] - b,\ x[k] = x[k] + b. \end{aligned} \qquad \textbf{[Eq. 19]}$$

$x[k]$ accumulates the error $\tilde{c}[k]$. If $x[k]$ becomes larger than $0.5b$, b is added to $\hat{c}[k]$ (compensation) and subtracted from $x[k]$ (for new error accumulation). If $x[k]$ becomes smaller than $-0.5b$, b is subtracted from $\hat{c}[k]$ and added to $x[k]$.

By using this mechanism, a very accurate control of the VCXO (which is critical to proper operation of the loop) is obtained with no need for a complex, expensive DAC. Correction is calculated continuously, and the control voltage to the VCXO is updated at the right timing, so as to obtain an accurate phase. Moreover, intensive digital implementation improves the temperature stability and power consumption of the VCXO control circuitry.

According to a preferred embodiment of the present invention, the method for BTR and error signal generation in blind mode employs a modification of Band-Edge Timing Recovery (BETR) method. Looking back at Fig. 5A, an algorithm for extracting the TRL phase error is described:

1) The incoming signal is sampled, demodulated, passes filters 13 and 14 and the resulting complex (I and Q) signal is fed to TRL 40. The resulting complex signal is given by:

$$z_r[n] + jz_i[n] \qquad \textbf{[Eq. 20]}$$

2) This signal has bandwidth from $-0.5(1+\alpha)f_b$ to $0.5(1+\alpha)f_b$, where f_b is the symbol rate and α is the bandwidth excess ratio. Therefore, the two band-edge components (base-band components at upper and lower frequencies) spectral lines can be recovered

by multiplying the demodulated complex signal z[n] by $\exp(j\pi f_b t)$ and $\exp(-j\pi f_b t)$.

According to a preferred embodiment of the invention, the sampling rate in blind mode is done at twice the symbol rate f_b. This method is known as Fractional Spaced Equalization (FSE), which is utilized for reducing the line amplitude and delay distortions appearing when the signal is sampled at the symbol rate.

Since the sampling frequency is $2f_b$, the signal is multiplied by the discrete-time sequences $\exp(j0.5\pi n)$ and $\exp(-j0.5\pi n)$. These sequences are very simple since the only possible values are 1, j, -1, $-j$. Therefore, the band-edge components can be formed without any multiplication, which is one of the main advantages of the present invention. The lower band edge component is given by:

$$\lambda_r[n]+j\lambda_i[n] \qquad \textbf{[Eq. 21]}$$

The upper band edge component is given by:

$$\mu_r[n]+j\mu_i[n] \qquad \textbf{[Eq. 22]}$$

where

$$\begin{aligned}
&\lambda_r[n]=z_r[n]\cos(0.5\pi n)-z_i[n]\sin(0.5\pi n),\\
&\lambda_i[n]=z_i[n]\cos(0.5\pi n)+z_r[n]\sin(0.5\pi n),\\
&\mu_r[n]=z_r[n]\cos(0.5\pi n)+z_i[n]\sin(0.5\pi n),\\
&\mu_i[n]=z_i[n]\cos(0.5\pi n)-z_r[n]\sin(0.5\pi n),
\end{aligned}
\qquad
\begin{aligned}
&\cos(0.5\pi n)=\ldots,1,0,-1,0,\ldots\\
&\sin(0.5\pi n)=\ldots,0,1,0,-1,\ldots
\end{aligned}
\qquad \textbf{[Eq. 23]}$$

Each of the components $\lambda_r[n]$, $\lambda_i[n]$, $\mu_r[n]$, $\mu_i[n]$ is filtered by LPF 21, 22, 23 and 24 respectively, forming a set of filtered values: $\overline{\lambda}_r[n]$, $\overline{\lambda}_i[n]$, $\overline{\mu}_r[n]$, $\overline{\mu}_i[n]$.

These values are multiplied and summed by the spectral line computer 25, and then

filtered again by LPF 26 and 27 respectively, in a way forming the I and Q component of the desired spectral line vector v[n]. Hence, the components of the spectral line vector $v[n] = v_r[n] + jv_i[n]$ are given by:

$$\begin{aligned} v_r[n] &= \overline{\lambda}_r[n]\overline{\mu}_r[n] + \overline{\lambda}_i[n]\overline{\mu}_i[n], \\ v_i[n] &= \overline{\lambda}_i[n]\overline{\mu}_r[n] - \overline{\lambda}_r[n]\overline{\mu}_i[n]. \end{aligned} \qquad \textbf{[Eq. 24]}$$

The phase of the spectral line vector is given by:

$$\tan^{-1}(v_i[n]/\, v_r[n]) \qquad \textbf{[Eq. 25]}$$

Since the phase error is small, the approximations $x \approx \sin x \approx tgx$ and $e(t) \approx \sin[\phi_{in}(t) - \phi(t)] \approx \phi_{in}(t) - \phi(t)$ may be used. Therefore, the phase error of the timing loop is proportional to $v_i[n]$. The proportionality factor is a function of the signal amplitude which may vary. Therefore, $v[n] = v_r[n] + jv_i[n]$ is fed to an amplitude normalizer 28, which normalizes the magnitude of $v_r[n] + jv_i[n]$ to be 1. This normalization is achieved by a widely used Automatic Gain Control (AGC) circuitry. After normalization, the normalized imaginary part of the spectral line, which is the required error signal of the loop, is sampled again at the symbol rate f_b, and fed to the controller 29 to lock the loop. From this point, blind equalization is performed until symbol error rate of less than 10^{-3} (or any other desired error rate) is achieved. Using the preferred embodiment of the present invention described above, blind equalization is accomplished in less than 0.1 Sec.

All the LPFs of TRL 40 are first-order Infinite Impulse Response (IIR) filters. Fig. 5B is a block-diagram of this filter, and its mathematical representation is given at Eq. 14 above. Going back to the Z domain, the output $Y(z)$ is multiplied by (1-a), time shifted by T, and added to the input $X(z)$ multiplied by a. According to the invention, a is

selected to be $a = 2^{-k}$ (k is an integer), leading to the filter's difference equation:

$$y[n] = y[n\text{-}1] + 2^{-k}*(x[n]\text{-}y[n\text{-}1]) \qquad \textbf{[Eq. 26]}$$

Since 2^{-k} is equivalent to a time-shift k, each LPF may be realized with no need for any multiplication.

According to a preferred embodiment of the present invention, a reduced constellation is transmitted by the master modem for the blind mode operation. This reduced constellation comprises only four symbols, each having the same amplitude. This method simplifies the equalization during blind mode, since the symbols differ from each other only in their phase. After equalization using reduced constellation, the line characteristics has been "extracted" and full constellation is started.

After blind equalization, the slave modem switches to the well known DDTR mode, as mentioned above. The operation of this mode is illustrated in Fig. 8, in which a 16 QAM constellation is presented. If there is any offset between the clock frequencies of the master and slave modems, phase error is generated, shifting the phase of any symbol in time. This shift is illustrated by arrows pointing towards the shifting direction of the phase. These phase shifts are detected by measuring the deviations of pre-detected symbols to from their post-detected symbols, and as a result the loop is adjusted to shift the VCXO frequency to the direction that minimizes the clusters that are generated around each state of the constellation. Since blind equalization has been already implemented, these clusters are relatively small, and the DDTR mode is utilized to maintain only fine corrections.

All the above description and examples have been provided for the purpose of illustration, and are not intended to limit the invention any way. Many modifications and additional operations can be effected in the method, and many different hardware elements, wiring and components can be used, all without exceeding the scope of the invention.

Claims

1. A method for the fast, timing recovery of transmitted data between two $\mathcal{X}$DSL modems, said data is transferred along a noisy, high loss, high distortion wiring, characterized by that data received at the slave modem as a sequence of symbols, is sampled at the symbol rate, converted to digital form, said sampled data been split to In-phase (I) and Quadrature (Q) channels, filtered with a digital Low-Pass Filter (LPF), sampled again at twice the symbol rate, and modulated each with the two discrete-time sequences

$$\cos(0.5\pi n) = \ldots,1,0,-1,0,\ldots$$
$$\sin(0.5\pi n) = \ldots,0,1,0,-1,\ldots$$

2. A method according to claim 1, comprising the steps of:

a) Providing a master $\mathcal{X}$DSL modem, synchronized by its own timing clock, for data transmission to a second slave $\mathcal{X}$DSL modem;

b) Providing a second slave $\mathcal{X}$DSL modem, synchronized by its own timing clock, for data reception from said master $\mathcal{X}$DSL modem;

c) Providing a communication wiring connecting said master modem to said slave modem;

d) Encoding and transmitting the desired data as a sequence of symbols to the slave modem using pre-determined QAM states;

e) Receiving the transmitted symbols at the slave receiver (demodulator);

f) Sampling the received signal;

g) Splitting the sampled data to in-phase (I) and quadrature (Q) channels;

h) Filtering each channels of step g) above with digital low-pass filters, said filters

being matched to the transmitting filters at the master modem;

i) Turning the master clock timing recovery into blind mode, by the steps of:

(1) Sampling the filtered I and Q outputs at twice the symbol rate;

(2) Extracting the lower and upper band edge components by modulating each of the sampled sequence of I and Q outputs of step (1) above with two discrete time sequences: $\begin{matrix}\cos(0.5\pi n)=\ldots,1,0,-1,0,\ldots \\ \sin(0.5\pi n)=\ldots,0,1,0,-1,\ldots\end{matrix}$;

(3) Filtering the four resulting products with four first order low-pass filters and re-sampling the results at the symbol rate;

(4) Computing the real and imaginary parts of the spectral line vector using the products of step (3) above;

(5) Filtering both the real and the imaginary parts of step (4) above, using another first order low-pass filter;

(6) Normalizing the magnitude of the spectral line vector to unity using a suitable automatic gain control circuitry;

(7) Extracting the phase of the spectral line vector from the normalized imaginary part of step (6) above;

(8) Feeding the sampled imaginary part of step (7) above as a phase-error signal to a controller of a phase-locked loop (PLL), said PLL utilizing a frequency controlled clock oscillator, the frequency of which is tuned to track the frequency of the incoming symbols (the master modem clock frequency);

(9) Converting the digital control word to analog control voltage supplied to the tracking oscillator of step (8) above, using a Digital to Analog Converter (DAC); and

(10) Using a secondary accumulator to correct the control word supplied to the DAC of step (9) above;

j) Feeding the I and Q filtered outputs to a complex linear equalizer for coarse phase and amplitude error correction;

k) Computing the symbol state data decisions using a slicer circuitry;

l) Fine equalization of the channel distortions by feeding the I and Q outputs of the slicer to a decision feedback equalizer, the outputs of which are extracted from the slicer I and Q inputs, respectively;

m) Computing the extracted symbols error rate at the slicer outputs; and

n) After the error probability decreases to a given BER, switching from blind mode timing recovery to data directed timing recovery mode.

3. A method according to claims 1 and 2, wherein the transmission medium is a pair of copper wires.

4. A method according to any one of claims 1 to 3, wherein the pair of copper wires is a telephone line.

5. A method according to claims 1 and 2 wherein the sampling rate is more than twice the symbol rate.

6. A method according to claims 1 and 2, wherein the timing oscillator utilized by the phase-locked loop is a Voltage-Controlled Crystal Oscillator (VCXO) or the like suitable clock oscillator.

7. A method according to any one of claims 1 to 6, wherein the blind timing recovery is achieved using a reduced constellation.

8. A method according to claim 7, wherein the reduced constellation comprises only equal amplitude symbols.

9. A method according to claim 1 to 6, wherein the blind timing recovery is achieved using full constellation.

10. A method according to claim 1 and 2, wherein the control signal of the PLL tracking oscillator is provided accurately and converted using an up to 8 bit Digital to Analog Converter (DAC) means, comprising the steps of:

a) Rounding the double precision control signal;

b) Generating an error signal between the double precision value and the rounded value;

c) Accumulating the error signal in a secondary accumulator;

d) Adding the error signal to the output signal of the secondary accumulator;

e) Comparing the result of step d) above with half the value of the DAC's LSB;

f) Compensating the rounded value according to the result of step e) above by the steps of:

(1) Adding the value of the DAC's LSB to the accumulator output, if the output value is larger than half the value of the DAC's LSB;or

(2) Subtracting the value of the DAC's LSB from the accumulator output, if the output value is smaller than half the value of the DAC's LSB;

11. A method according to any one of claims 1 to 10, substantially as described and illustrated.

12. An $\mathcal{X}$DSL modem for fast timing recovery of received data, said data transmitted between two $\mathcal{X}$DSL modems and transferred trough a noisy, high loss, high distortion wiring, comprising:

a) Circuitry for receiving the transmitted symbols at the slave receiver (demodulator);

b) Circuitry for sampling the received signal;

c) Circuitry for splitting the sampled data to in-phase (I) and quadrature (Q) channels;

d) Circuitry for filtering each channels of step c) above with digital low-pass filters, said filters being matched to the transmitting filters at the master modem;

e) Circuitry for turning the master clock timing recovery into blind mode, by the steps of:

(1) Circuitry for sampling the filtered I and Q outputs at twice the symbol rate;

(2) Circuitry for extracting the lower and upper band edge components by modulating each of the sampled sequence of I and Q outputs of step (1) above with two discrete time sequences: $\begin{matrix}\cos(0.5\pi n)=\ldots,1,0,-1,0,\ldots \\ \sin(0.5\pi n)=\ldots,0,1,0,-1,\ldots\end{matrix}$;

(3) Circuitry for filtering the four resulting products with four first order low-

pass filters and re-sampling the results at the symbol rate;

(4) Circuitry for computing the real and imaginary parts of the spectral line vector using the products of step (3) above;

(5) Circuitry for filtering both the real and the imaginary parts of step (4) above, using one or more first order low-pass filter;

(6) Circuitry for normalizing the magnitude of the spectral line vector to unity using a suitable automatic gain control circuitry;

(7) Circuitry for extracting the phase of the spectral line vector from the normalized imaginary part of step (6) above;

(8) Circuitry for feeding the sampled imaginary part of step (7) above as a phase-error signal to a controller of a phase-locked loop (PLL), said PLL utilizing a frequency controlled clock oscillator, the frequency of which is tuned to track the frequency of the incoming symbols (the master modem clock frequency);

(9) Circuitry for converting the digital control word to analog control voltage supplied to the tracking oscillator of step (8) above, using a Digital to Analog Converter (DAC).

f) Circuitry for feeding the I and Q filtered outputs to a complex linear equalizer for coarse phase and amplitude error correction;

g) Circuitry for computing the symbol state data decisions using a slicer circuitry;

h) Fine equalizing the channel distortions by feeding the I and Q outputs of the slicer to a decision feedback equalizer, the outputs of which is extracted from the slicer I and Q inputs, respectively;

i) Circuitry for computing the extracted symbols error rate at the slicer outputs; and

j) Circuitry for switching from blind mode timing recovery to data directed timing recovery mode, once the error is reduced to less than a given BER.

13. A modem according to claim 12, further comprising (10) circuitry for accumulation to correct the control word supplied to the DAC by providing:

a) Circuitry for rounding the double precision control signal;

b) Circuitry for generation of an error signal between the double precision value and the rounded value;

c) Circuitry for accumulation of the error signal in a secondary accumulator;

d) Circuitry for adding the error signal to the output signal of the secondary accumulator;

e) Circuitry for comparing the result of step (d) above with half the value of the DAC's LSB;

f) Circuitry for compensating the rounded value according to the result of step (e) above and by:

(1) Circuitry for adding the value of the DAC's LSB to the accumulator output, if the output value is larger than half the value of the DAC's LSB; and

(2) Circuitry for subtracting the value of the DAC's LSB from the accumulator output, if the output value is smaller than half the value of the DAC's LSB;

14. A modem according to claim 12, comprising means for sampling at a sampling rate that is more than twice the symbol rate.

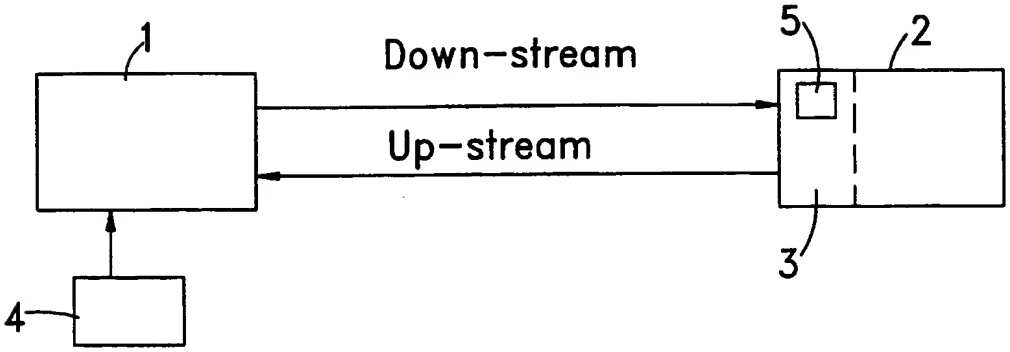

1
Down-stream
5
2
Up-stream
3
4

Fig. 1

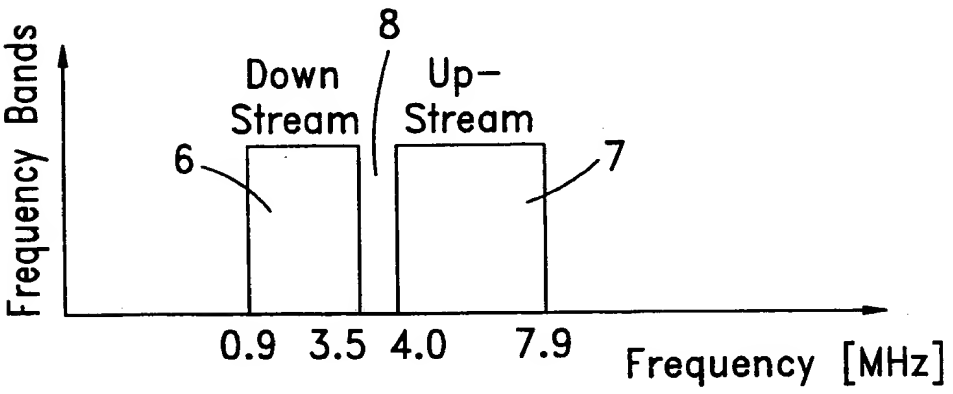

8
Down Stream
Up- Stream
6
7
Frequency Bands
0.9
3.5
4.0
7.9
Frequency [MHz]

Fig. 2A

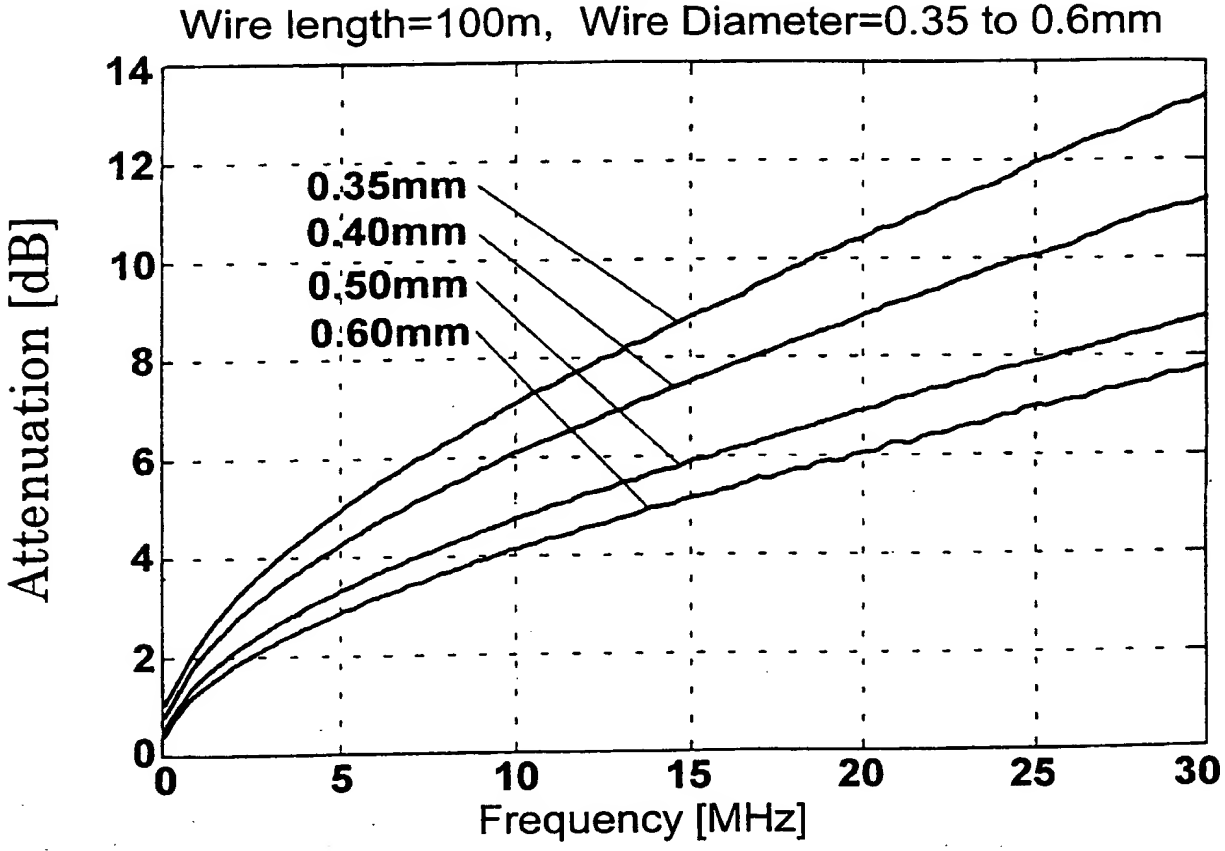

Wire length=100m, Wire Diameter=0.35 to 0.6mm
Attenuation [dB]
0.35mm
0.40mm
0.50mm
0.60mm
Frequency [MHz]
0
2
4
6
8
10
12
14
0
5
10
15
20
25
30

Fig. 2B

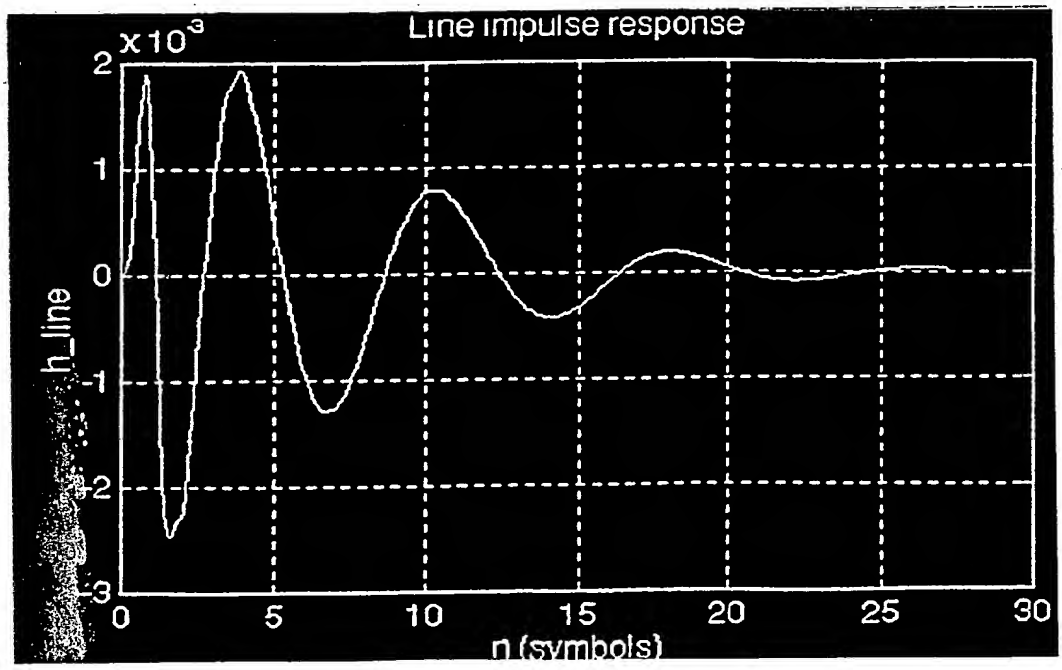

Line impulse response
x 10^-3
h_line
n (symbols)
2
1
0
-1
-2
-3
0
5
10
15
20
25
30

Fig. 3

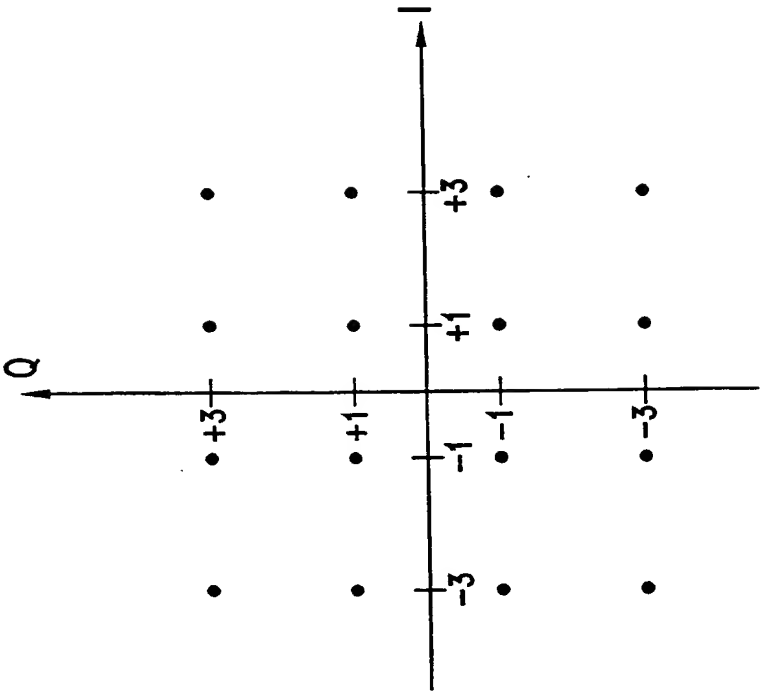
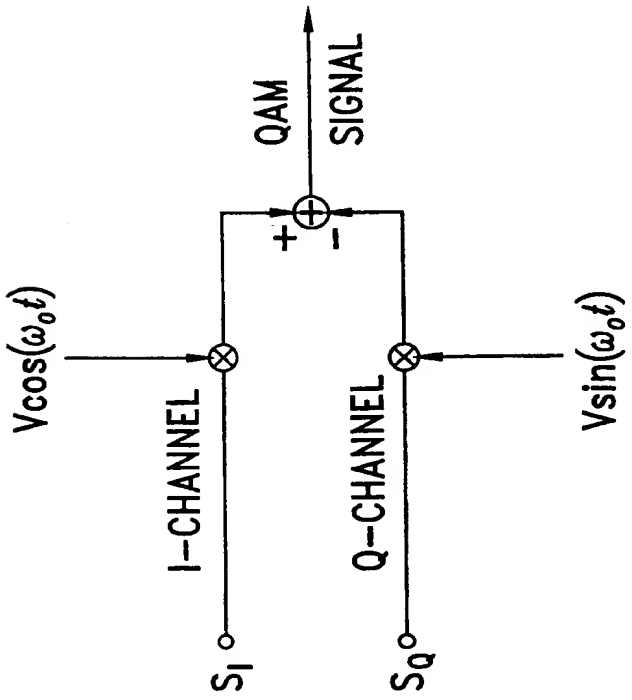

I
Q
+3
+1
-1
-3
+3
+1
-1
-3

Fig. 4


QAM SIGNAL
+
-
Vcos(ω₀t)
Vsin(ω₀t)
I-CHANNEL
Q-CHANNEL
SI
SQ

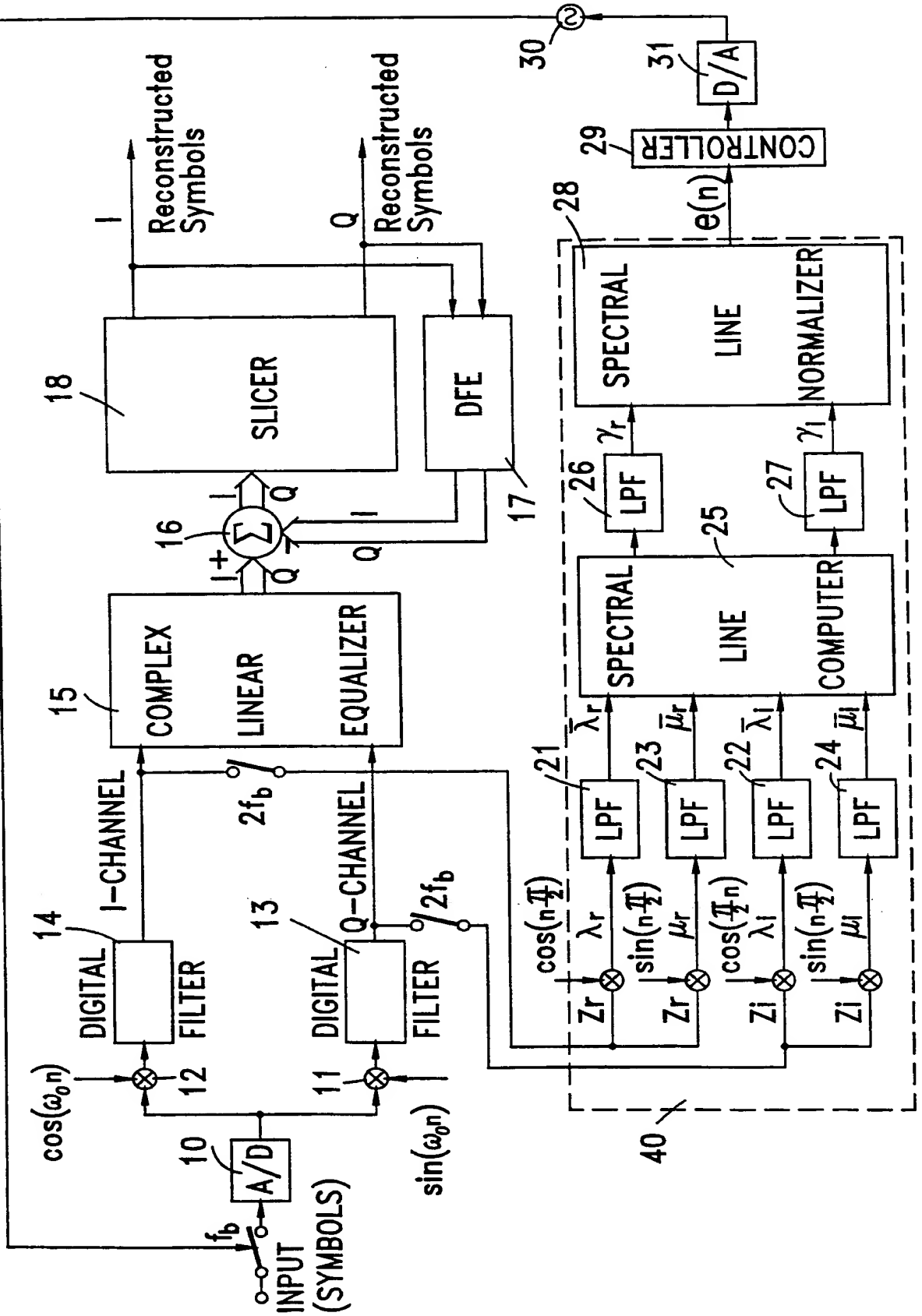

SAMPLING RATE
INPUT (SYMBOLS)
A/D
10
f_b
$\cos(\omega_0 n)$
$\sin(\omega_0 n)$
12
11
DIGITAL FILTER
14
13
I-CHANNEL
Q-CHANNEL
$2f_b$
15
COMPLEX LINEAR EQUALIZER
16
17
SLICER
18
DFE
I
Q
Reconstructed Symbols
30
31
D/A
CONTROLLER
29
e(n)
28
SPECTRAL LINE NORMALIZER
γ_r
γ_i
26
27
LPF
25
SPECTRAL LINE COMPUTER
$\bar{\lambda}_r$
$\bar{\mu}_r$
$\bar{\lambda}_i$
$\bar{\mu}_i$
21
23
22
24
$\cos(n\frac{\pi}{2})$
$\sin(n\frac{\pi}{2})$
$\cos(\frac{\pi}{2}n)$
$\sin(n\frac{\pi}{2})$
λ_r
μ_r
λ_i
μ_i
Zr
Zi
40

Fig. 5A

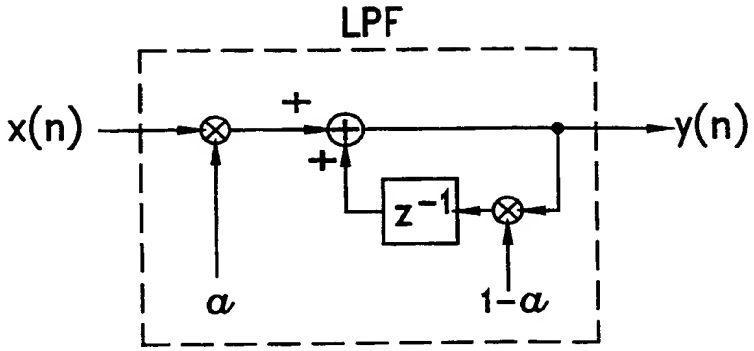


Fig. 5B

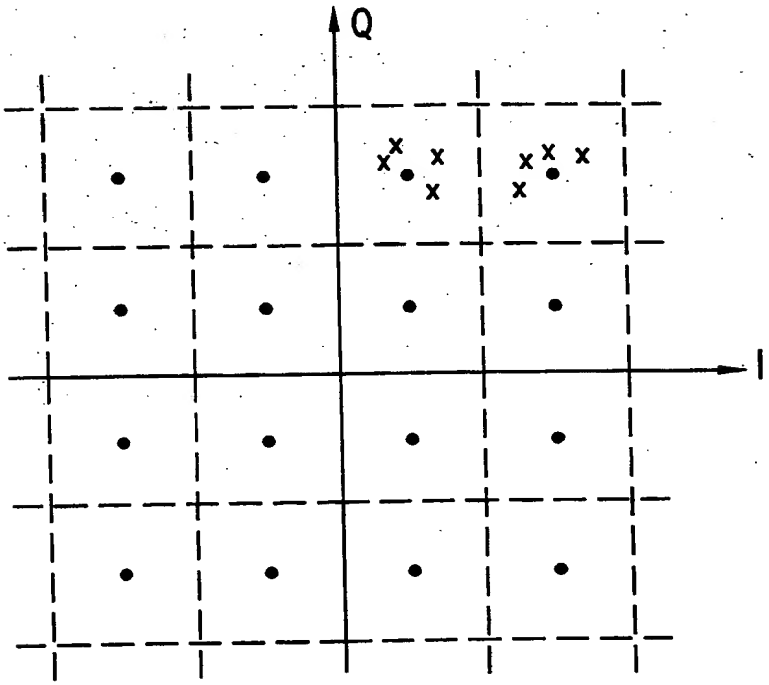


Fig. 6

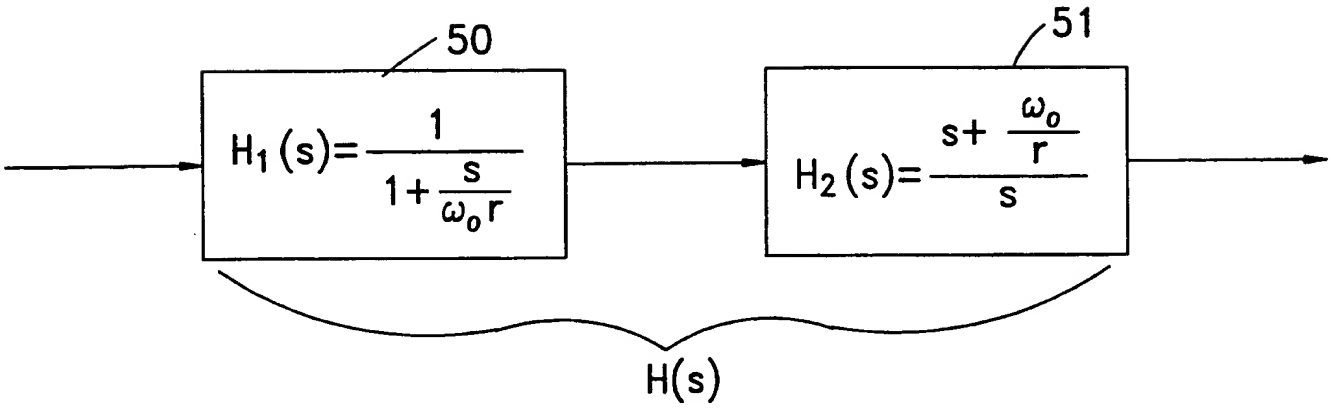


Fig. 7

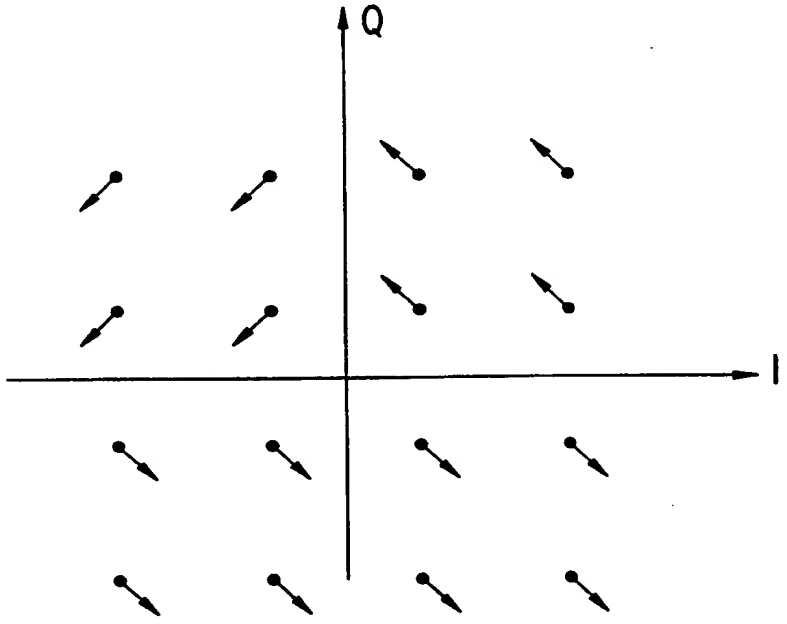


Fig. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IL99/00154

A. CLASSIFICATION OF SUBJECT MATTER
IPC(6) : H04B 1/38, 1/50; H04L 5/12, 5/16
US CL : 375/222, 261, 350
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 375/222, 223, 261, 350, 355; 379/93.09; 370/493, 494, 495

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS searched terms: ?dsl modem#

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5,163,044 A (GOLDEN) 10 November 1992, abstract, figures 3-4 and col. 2, lines 6-41.	1-14
A	US 5,222,077 A (KRISHNAN) 22 June 1993, abstract.	1-14
A	US 5,331,670 A (SORBARA et al) 19 July 1994, abstract and figure 6.	1-14

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search	Date of mailing of the international search report
28 JUNE 1999	17 AUG 1999
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer DON N VO James R. Matthews Telephone No. (703) 305-4885

Form PCT/ISA/210 (second sheet)(July 1992)*

PATENT COOPERATION TREATY

PCT

corrected

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference 4650/WO/98	FOR FURTHER ACTION	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
International application No. PCT/IL99/00154	International filing date *(day/month/year)* 18 MARCH 1999	Priority date *(day/month/year)* 19 MARCH 1998
International Patent Classification (IPC) or national classification and IPC IPC(6): H04B 1/38, 1/50; H04L 5/12, 5/16 and US Cl.: 375/222, 261, 350		
Applicant SAVAN COMMUNICATIONS LTD.		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 4 sheets.

   [1] This report is also accompanied by ANNEXES, i.e., sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority. (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 3 sheets.

3. This report contains indications relating to the following items:

   I [X] Basis of the report

   II [ ] Priority

   III [ ] Non-establishment of report with regard to novelty, inventive step or industrial applicability

   IV [ ] Lack of unity of invention

   V [X] Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

   VI [ ] Certain documents cited

   VII [ ] Certain defects in the international application

   VIII [X] Certain observations on the international application

Date of submission of the demand	Date of completion of this report
27 SEPTEMBER 1999	23 MAY 2000
Name and mailing address of the IPEA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer DON N VO Telephone No. (703) 305-4885

Form PCT/IPEA/409 (cover sheet) (July 1998) ★

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/IL99/00154

I. Basis of the report

1. With regard to the elements of the international application:*

☐ the international application as originally filed

☒ the description:
pages (See Attached), as originally filed
pages _____, filed with the demand
pages _____, filed with the letter of _____

☒ the claims:
pages (See Attached), as originally filed
pages _____, as amended (together with any statement) under Article 19
pages _____, filed with the demand
pages _____, filed with the letter of _____

☒ the drawings:
pages (See Attached), as originally filed
pages _____, filed with the demand
pages _____, filed with the letter of _____

☒ the sequence listing part of the description:
pages (See Attached), as originally filed
pages _____, filed with the demand
pages _____, filed with the letter of _____

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.
These elements were available or furnished to this Authority in the following language _____ which is:

☐ the language of a translation furnished for the purposes of international search (under Rule 23.1(b)).

☐ the language of publication of the international application (under Rule 48.3(b)).

☐ the language of the translation furnished for the purposes of international preliminary examination (under Rules 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

☐ contained in the international application in printed form.

☐ filed together with the international application in computer readable form.

☐ furnished subsequently to this Authority in written form.

☐ furnished subsequently to this Authority in computer readable form.

☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

☐ The statement that the information recorded in computer readable form is identical to the writen sequence listing has been furnished.

4. ☒ The amendments have resulted in the cancellation of:

☒ the description, pages NONE

☒ the claims, Nos. NONE

☒ the drawings, sheets/~~fig~~ NONE

5. ☒ This report has been drawn as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).**

** Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17).*

***Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.*

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/IL99/00154

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. statement

Novelty (N)	Claims	1-14	YES
	Claims	NONE	NO
Inventive Step (IS)	Claims	1-14	YES
	Claims	NONE	NO
Industrial Applicability (IA)	Claims	1-14	YES
	Claims	NONE	NO

2. citations and explanations (Rule 70.7)

Claims 1-14 meet the criteria set out in PCT Article 33(2)-(4), because the prior art does not teach or fairly suggest, in combination, the arrangements of the data received at the slave modem as a sequence of symbols, is sampled at the symbol rate, converted to digital form, said sampled data been split to In-phase (I) and Quadrature (Q) channels, filtered with a digital Low-Pass Filter (LPF), sampled again at twice the symbol rate, and modulated each with the two discrete-time sequences in order to form a method for the fast, timing recovery of transmitted data between two XDSL modems as recited in claim 1 and variations of circuit arrangements as recited in claim 12 and further limitations of their respective dependent claims 2-11 and 13-14.

---------- NEW CITATIONS ----------

NONE

Supplemental Box
(To be used when the space in any of the preceding boxes is not sufficient)

Continuation of: Boxes I - VIII

I. BASIS OF REPORT:

This report has been drawn on the basis of the description,
page(s) 1-25, as originally filed.
page(s) NONE, filed with the demand.
and additional amendments:
NONE

This report has been drawn on the basis of the claims,
page(s) 26-29, as originally filed.
page(s) NONE, as amended under Article 19.
page(s) NONE, filed with the demand.
and additional amendments:
Pages 30-32, filed with the letter of 09 March 2000.

This report has been drawn on the basis of the drawings,
page(s) 1-6, as originally filed.
page(s) NONE, filed with the demand.
and additional amendments:
NONE

This report has been drawn on the basis of the sequence listing part of the description:
page(s) NONE, as originally filed.
pages(s) NONE, filed with the demand.
and additional amendments:
NONE

5. (Some) amendments are considered to go beyond the disclosure as filed:
NONE

(2) Subtracting the value of the DAC's LSB from the accumulator output, if the output value is smaller than half the value of the DAC's LSB;

11. A method according to any one of claims 1 to 10, substantially as described and illustrated.

12. An $\mathcal{X}$DSL modem for fast timing recovery of received data, said data transmitted between two $\mathcal{X}$DSL modems and transferred trough a noisy, high loss, high distortion wiring, comprising:

a) Circuitry for receiving the transmitted symbols at the slave receiver (demodulator);

b) Circuitry for sampling the received signal;

c) Circuitry for splitting the sampled data to in-phase (I) and quadrature (Q) channels;

d) Circuitry for filtering each channels of step c) above with digital low-pass filters, said filters being matched to the transmitting filters at the master modem;

e) Circuitry for turning the master clock timing recovery into blind mode, by the steps of:

(1) Circuitry for sampling the filtered I and Q outputs at twice the symbol rate;

(2) Circuitry for extracting the lower and upper band edge components by modulating each of the sampled sequence of I and Q outputs of step (1) above with two discrete time sequences: $\begin{matrix}\cos(0.5\pi n)=\ldots,1,0,-1,0,\ldots \\ \sin(0.5\pi n)=\ldots,0,1,0,-1,\ldots\end{matrix}$;

(3) Circuitry for filtering the four resulting products with four first order low-

REPLACED BY ART 34 AMDT

pass filters and re-sampling the results at the symbol rate;

(4) Circuitry for computing the real and imaginary parts of the spectral line vector using the products of step (3) above;

(5) Circuitry for filtering both the real and the imaginary parts of step (4) above, using one or more first order low-pass filter;

(6) Circuitry for normalizing the magnitude of the spectral line vector to unity using a suitable automatic gain control circuitry;

(7) Circuitry for extracting the phase of the spectral line vector from the normalized imaginary part of step (6) above;

(8) Circuitry for feeding the sampled imaginary part of step (7) above as a phase-error signal to a controller of a phase-locked loop (PLL), said PLL utilizing a frequency controlled clock oscillator, the frequency of which is tuned to track the frequency of the incoming symbols (the master modem clock frequency);

(9) Circuitry for converting the digital control word to analog control voltage supplied to the tracking oscillator of step (8) above, using a Digital to Analog Converter (DAC).

f) Circuitry for feeding the I and Q filtered outputs to a complex linear equalizer for coarse phase and amplitude error correction;

g) Circuitry for computing the symbol state data decisions using a slicer circuitry;

h) Fine equalizing the channel distortions by feeding the I and Q outputs of the slicer to a decision feedback equalizer, the outputs of which is extracted from the slicer I and Q inputs, respectively;

i) Circuitry for computing the extracted symbols error rate at the slicer outputs; and

j) Circuitry for switching from blind mode timing recovery to data directed timing recovery mode, once the error is reduced to less than a given BER.

13. A modem according to claim 12, further comprising (10) circuitry for accumulation to correct the control word supplied to the DAC by providing:

a) Circuitry for rounding the double precision control signal;

b) Circuitry for generation of an error signal between the double precision value and the rounded value;

c) Circuitry for accumulation of the error signal in a secondary accumulator;

d) Circuitry for adding the error signal to the output signal of the secondary accumulator;

e) Circuitry for comparing the result of step (d) above with half the value of the DAC's LSB;

f) Circuitry for compensating the rounded value according to the result of step (e) above and by:

(1) Circuitry for adding the value of the DAC's LSB to the accumulator output, if the output value is larger than half the value of the DAC's LSB; and

(2) Circuitry for subtracting the value of the DAC's LSB from the accumulator output, if the output value is smaller than half the value of the DAC's LSB;

14. A modem according to claim 12, comprising means for sampling at a sampling rate that is more than twice the symbol rate.

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

16

Applicant's or agent's file reference 4650/WO/98	FOR FURTHER ACTION	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
International application No. PCT/IL99/00154	International filing date *(day/month/year)* 18 MARCH 1999	Priority date *(day/month/year)* 19 MARCH 1998
International Patent Classification (IPC) or national classification and IPC IPC(6): H04B 1/38, 1/50; H04L 5/12, 5/16 and US Cl.: 375/222, 261, 350		
Applicant SAVAN COMMUNICATIONS LTD.		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 5 sheets.

   ☐ This report is also accompanied by ANNEXES, i.e., sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority. (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 0 sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the report
   - II ☐ Priority
   - III ☐ Non-establishment of report with regard to novelty, inventive step or industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
   - VI ☐ Certain documents cited
   - VII ☐ Certain defects in the international application
   - VIII ☒ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
27 SEPTEMBER 1999	23 MAY 2000
Name and mailing address of the IPEA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer DON N VO James R. Matthews Telephone No. (703) 305-4885

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/IL99/00154

I. Basis of the report

1. With regard to the **elements** of the international application:*

[X] the international application as originally filed

[X] the description:
pages 1-25 , as originally filed
pages NONE , filed with the demand
pages NONE , filed with the letter of _____

[X] the claims:
pages 26-32 , as originally filed
pages NONE , as amended (together with any statement) under Article 19
pages NONE , filed with the demand
pages NONE , filed with the letter of _____

[X] the drawings:
pages 1-6 , as originally filed
pages NONE , filed with the demand
pages NONE , filed with the letter of _____

[X] the sequence listing part of the description:
pages NONE , as originally filed
pages NONE , filed with the demand
pages NONE , filed with the letter of _____

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.
These elements were available or furnished to this Authority in the following language _____ which is:

[ ] the language of a translation furnished for the purposes of international search (under Rule 23.1(b)).

[ ] the language of publication of the international application (under Rule 48.3(b)).

[ ] the language of the translation furnished for the purposes of international preliminary examination (under Rules 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

[ ] contained in the international application in printed form.

[ ] filed together with the international application in computer readable form.

[ ] furnished subsequently to this Authority in written form.

[ ] furnished subsequently to this Authority in computer readable form

[ ] The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

[ ] The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. [X] The amendments have resulted in the cancellation of:

[X] the description, pages NONE

[X] the claims, Nos. NONE

[X] the drawings, sheets/fig NONE

5. [X] This report has been drawn as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).**

** Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17).*

***Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.*

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/IL99/00154

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. statement

Novelty (N)	Claims	1-14	YES
	Claims	NONE	NO
Inventive Step (IS)	Claims	1-14	YES
	Claims	NONE	NO
Industrial Applicability (IA)	Claims	1-14	YES
	Claims	NONE	NO

2. citations and explanations (Rule 70.7)

Claims 1-14 meet the criteria set out in PCT Article 33(2)-(4), because the prior art does not teach or fairly suggest, in combination, the arrangements of the data received at the slave modem as a sequence of symbols, is sampled at the symbol rate, converted to digital form, said sampled data been split to In-phase (I) and Quadrature (Q) channels, filtered with a digital Low-Pass Filter (LPF), sampled again at twice the symbol rate, and modulated each with the two discrete-time sequences in order to form a method for the fast, timing recovery of transmitted data between two XDSL modems as recited in claim 1 and variations of circuit arrangements as recited in claim 12 and further limitations of their respective dependent claims 2-11 and 13-14.

---------- NEW CITATIONS ----------

NONE

VIII. Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

Claims 10-14 are objected to under PCT Rule 66.2(a)(v) as lacking clarity under PCT Article 6 because the claims indefinite for the following reason(s):

Claim 10 appears to be incomplete because it is ended with a semicolon (;). Similar problem exists for claim 13.

Claim 12, line 34 (page 31, line 17) ends with a period. It is unclear whether the remaining steps f through j includes in the claim.

Supplemental Box
(To be used when the space in any of the preceding boxes is not sufficient)

Continuation of: Boxes I - VIII

I. BASIS OF REPORT:

5. (Some) amendments are considered to go beyond the disclosure as filed:
NONE

PCT

REQUEST

The undersigned requests that the present international application be processed according to the Patent Cooperation Treaty

For receiving Office use only

International Application No.

International Filing Date

Name of receiving Office and "PCT International Application"

Applicant's or agent's file reference
(if desired) (12 characters maximum) 4650/WO/98

Box No. I TITLE OF INVENTION
METHOD AND APPARATUS FOR CLOCK TIMING RECOVERY IN *X*DSL, PARTICULARLY VDSL MODEMS

Box No. II APPLICANT

Name and address:

SAVAN COMMUNICATIONS LTD.
71a Hamelacha Street
Netanya 42504
Israel

☐ This person is also an inventor.

Telephone No.

Facsimile No.

Teleprinter No.

State *(i.e. country)* of nationality: IL

State *(i.e. country)* of residence: IL

This person is applicant for the purposes of: ☐ all designated States ☒ all designated States except the United States of America ☐ the United States of America only ☐ the States indicated in the Supplemental Box

Box No. III FURTHER APPLICANT(S) AND/OR (FURTHER) INVENTOR(S)

Name and address:

PORAT, Boaz
93 Shimshon Street
Haifa 34678
Israel

This person is:
☐ applicant only
☒ applicant and inventor
☐ inventor only

State *(i.e. country)* of nationality:IL

State *(i.e. country)* of residence:IL

This person is applicant for the purposes of: ☐ all designated States ☐ all designated States except the United States of America ☒ the United States of America only ☐ the States indicated in the Supplemental Box

☒ Further applicants and/or (further) inventors are indicated on a continuation sheet

Box No. IV AGENT OR COMMON REPRESENTATIVE; OR ADDRESS FOR CORRESPONDENCE

The person identified below is hereby/has been appointed to act on behalf of the applicant(s) before the competent International Authorities as: ☒ agent ☐ common representative

Name and address:

LUZZATTO, Kfir
LUZZATTO & LUZZATTO
P.O.Box 5352
Beer-Sheva 84 152
Israel

Telephone No.
(972-7) 6497-871

Facsimile No.
(972-7) 6497-125

Teleprinter No.

☐ Mark this check-box where no agent or common representative is/has been appointed and the space above is used instead to indicate a special address to which correspondence should be sent.

Continuation of Box No. III **FURTHER APPLICANT(S) AND/OR (FURTHER) INVENTOR(S)**

If none of the following sub-boxes is used, this sheet is not to be included in the request

Name and address:

HARPAK, Amnon
62 Moshe Dayan Street
Holon 58671
Israel

This person is:
☐ applicant only
☒ applicant and inventor
☐ inventor only

State *(i.e. country)* of nationality: IL

State *(i.e. country)* of residence: IL

This person is applicant for the purposes of: ☐ all designated States ☐ all designated States except the United States of America ☒ the United States of America only ☐ the States indicated in the Supplemental Box

Name and address:

PELEG, Shimon
11 Anchilevich Street
Hod-Hasharon 45285
Israel

This person is:
☐ applicant only
☒ applicant and inventor
☐ inventor only

State *(i.e. country)* of nationality: IL

State *(i.e. country)* of residence: IL

This person is applicant for the purposes of: ☐ all designated States ☐ all designated States except the United States of America ☒ the United States of America only ☐ the States indicated in the Supplemental Box

Name and address:

This person is:
☐ applicant only
☐ applicant and inventor
☐ inventor only

State *(i.e. country)* of nationality

State *(i.e. country)* of residence:

This person is applicant for the purposes of: ☐ all designated States ☐ all designated States except the United States of America ☐ the United States of America only ☐ the States indicated in the Supplemental Box

Name and address:

This person is:
☐ applicant only
☐ applicant and inventor
☐ inventor only

State *(i.e. country)* of nationality

State *(i.e. country)* of residence:

This person is applicant for the purposes of: ☐ all designated States ☐ all designated States except the United States of America ☐ the United States of America only ☐ the States indicated in the Supplemental Box

☐ Further applicants and/or (further) inventors are indicated on a continuation sheet

Box No. V DESIGNATION OF STATES

The following designations are hereby made under Rule 4.9(a) *(mark the applicable check-boxes; at least one must be marked):*

Regional Patent

☒ **AP** **ARIPO Patent: GH** Ghana, **GM** Gambia, **KE** Kenya, **LS** Lesotho, **MW** Malawi, **SD** Sudan, **SZ** Swaziland, **UG** Uganda, **ZW** Zimbabwe, and any other State which is a Contracting State of the Harare Protocol and of the PCT

☒ **EA** **Eurasian Patent: AM** Armenia, **AZ** Azerbaijan, **BY** Belarus, **KG** Kyrgyzstan, **KZ** Kazakhstan, **MD** Republic of Moldova, **RU** Russian Federation, **TJ** Tajikistan, **TM** Turkmenistan, and any other State which is a Contracting State of the Eurasian Patent Convention and of the PCT

☒ **EP** **European Patent: AT** Austria, **BE** Belgium, **CH and LI** Switzerland and Liechtenstein, **CY** Cyprus, **DE** Germany, **DK** Denmark, **ES** Spain, **FI** Finland, **FR** France, **GB** United Kingdom, **GR** Greece, **IE** Ireland, **IT** Italy, **LU** Luxembourg, **MC** Monaco, **NL** Netherlands, **PT** Portugal, **SE** Sweden, and any other State which is a Contracting State of the European Patent Convention and of the PCT

☒ **OA** **OAPI Patent: BF** Burkina Faso, **BJ** Benin, **CF** Central African Republic, **CG** Congo, **CI** Côte d'Ivoire, **CM** Cameroon, **GA** Gabon, **GN** Guinea, **GW** Guinea-Bissau, **ML** Mali, **MR** Mauritania, **NE** Niger, **SN** Senegal, **TD** Chad, **TG** Togo, and any other State which is a member State of OAPI and a Contracting State of the PCT *(if other kind of protection or treatment desired, specify on dotted line)* . . . . . .

National Patent *(If other kind of protection or treatment desired, specify on dotted line):*

☒	**AL**	Albania	☒	**LS**	Lesotho
☒	**AM**	Armenia	☒	**LT**	Lithuania
☒	**AT**	Austria	☒	**LU**	Luxembourg
☒	**AU**	Australia	☒	**LV**	Latvia
☒	**AZ**	Azerbaijan	☒	**MD**	Republic of Moldova
☒	**BA**	Bosnia and Herzegovina	☒	**MG**	Madagascar
☒	**BB**	Barbados	☒	**MK**	The former Yugoslav Republic of Macedonia
☒	**BG**	Bulgaria	☒	**MN**	Mongolia
☒	**BR**	Brazil	☒	**MW**	Malawi
☒	**BY**	Belarus	☒	**MX**	Mexico
☒	**CA**	Canada	☒	**NO**	Norway
☒	**CH and LI**	Switzerland and Liechtenstein	☒	**NZ**	New Zealand
☒	**CN**	China	☒	**PL**	Poland
☒	**CU**	Cuba	☒	**PT**	Portugal
☒	**CZ**	Czech Republic	☒	**RO**	Romania
☒	**DE**	Germany	☒	**RU**	Russian Federation
☒	**DK**	Denmark	☒	**SD**	Sudan
☒	**EE**	Estonia	☒	**SE**	Sweden
☒	**ES**	Spain	☒	**SG**	Singapore
☒	**FI**	Finland	☒	**SI**	Slovenia
☒	**GB**	United Kingdom	☒	**SK**	Slovakia
☒	**GD**	Grenada	☒	**SL**	Sierra Leone
☒	**GE**	Georgia	☒	**TJ**	Tajikistan
☒	**GH**	Ghana	☒	**TM**	Turkmenistan
☒	**GM**	Gambia	☒	**TR**	Turkey
☒	**HR**	Croatia	☒	**TT**	Trinidad and Tobago
☒	**HU**	Hungary	☒	**UA**	Ukraine
☒	**ID**	Indonesia	☒	**UG**	Uganda
☒	**IL**	Israel	☒	**US**	United States of America
☒	**IN**	India	☒	**UZ**	Uzbekistan
☒	**IS**	Iceland	☒	**VN**	Viet Nam
☒	**JP**	Japan	☒	**YU**	Yugoslavia
☒	**KE**	Kenya	☒	**ZW**	Zimbabwe
☒	**KG**	Kyrgyzstan			
☒	**KP**	Democratic People's Republic of Korea			
☒	**KR**	Republic of Korea			
☒	**KZ**	Kazakstan			
☒	**LC**	Saint Lucia			
☒	**LK**	Sri Lanka			
☒	**LR**	Liberia			

Check-boxes reserved for designating States (for the purposes of a national patent) which have become party to the PCT after issuance of this sheet:

☒	**AE**	United Arab Emirates
☒	**ZA**	South Africa
☐		

Precautionary Designation Statement: In addition to the designations made above, the applicant also makes under Rule 4.9(b) all other designations which would be permitted under the PCT except any designation(s) indicated in the Supplemental Box as being excluded from the scope of this statement. The applicant declares that those additional designations are subject to confirmation and that any designation which is not confirmed before the expiration of 15 months from the priority date is to be regarded as withdrawn by the applicant at the expiration of that time limit. *(Confirmation of a designation consists of the filing of a notice specifying that designation and the payment of the designation and confirmation fees. Confirmation must reach the receiving Office within the 15-month time limit.)*

Supplemental Box *If the supplemental Box is not used, this sheet need not be included in the request.*

Continuation of Box No. IV

LUZZATTO, Edgar

LUZZATTO, Esther

HACKMEY, Michal

FUERST, Zadok

PYERNIK, Moshe

MANZUROLA, Emanuel

MORAG, Tamar

PRICE, Eyal

SHALEV, Ronit

HACKMEY, Miriam

P.O.Box 5352
Beer-Sheva 84 152
Israel

Box No. VI PRIORITY CLAIM Further priority claims are indicated in the Supplemental Box ☐

The priority of the following earlier application(s) is hereby claimed:

Country *(in which, of for which the application was filed)*	Filing Date *(day/month/year)*	Application No.	Office of filing *(only for regional or international application)*
item(1) IL	19 March 1998 (19.03.98)	123739	
item(2)			
item(3)			

Mark the following check-box if the certified copy of the earlier application is to be issued by the Office which for the purposes of the present international application is the receiving Office (a fee may be required):

☒ The receiving Office is hereby requested to prepare and transmit to the International Bureau a certified copy of the earlier application(s) identified above as item(s): (1)

Box No. VII INTERNATIONAL SEARCHING AUTHORITY

Choice of International Searching Authority (ISA) *(If two or more International Searching Authorities are competent to carry out the international search, indicate the Authority chosen; the two-letter code may be used):* **ISA / US**

Earlier Search *Fill in where a search (international, international-type or ther) by the International Searching Authority has already been carried out or requested and the Authority is now requested to base the international search, to the extent possible, on the results of that earlier search. Identify such search or request either by reference to the relevant application (or the translation thereof) or by reference to the search request:*

Country (or regional Office): Date *(day/month/year)*: Number:

Box No. VIII CHECK LIST

This international application contains the following number of sheets:

1. request	:	5 sheets
2. description	:	25 sheets
3. claims	:	7 sheets
4. abstract	:	1 sheets
5. drawings:		6 sheets
Total	:	44 sheets

This International application is accompanied

1. ☐ separate signed power of attorney
2. ☐ copy of general power of attorney
3. ☐ statement explaining lack of signature
4. ☐ priority document(s) *identified in Box No. VI as item(s):*
5. ☒ fee calculation sheet
6. ☐ separate indications concerning deposited microorganisms
7. ☐ nucleotide and/or amino acid sequence listing (diskette)
8. ☐ other *(specify)*

Figure No. _____ of the drawings (if any) should accompany the abstract when it is published.

Box No. IX SIGNATURE OF APPLICANT OR AGENT

Next to each signature, indicate the name of the person signing and the capacity in which the person signs (if such capacity is not obvious from reading the request)

Zadok Fuerst

For receiving Office use only

1. Date of actual receipt of the purported international application:
2. Drawings: ☐ received: ☐ not received:
3. Corrected date of actual receipt due to later but timely received papers or drawings completing the purported international application:
4. Date of timely receipt of the required corrections under PCT Article 11(2):
5. International Searching Authority specified by the applicant: **ISA/**
6. ☐ Transmittal of search copy delayed until search fee is paid

For International Bureau use only

Date of receipt of the record copy by the International Bureau:

WO 99/48219
PCT/IL99/00154

PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

PCT

NOTICE INFORMING THE APPLICANT OF THE COMMUNICATION OF THE INTERNATIONAL APPLICATION TO THE DESIGNATED OFFICES

(PCT Rule 47.1(c), first sentence)

To:
LUZZATTO, Kfir
Luzzatto & Luzzatto
P.O. Box 5352
84152 Beer-Sheva
ISRAËL

Date of mailing (day/month/year) 23 September 1999 (23.09.99)	
Applicant's or agent's file reference 4650/WO/98	**IMPORTANT NOTICE**

International application No.	**International filing date** (day/month/year)	**Priority date** (day/month/year)
PCT/IL99/00154	18 March 1999 (18.03.99)	19 March 1998 (19.03.98)

Applicant
SAVAN COMMUNICATIONS LTD. et al

1. Notice is hereby given that the International Bureau has communicated, as provided in Article 20, the international application to the following designated Offices on the date indicated above as the date of mailing of this Notice:
   AU,CN,EP,IL,JP,KP,KR,US

   In accordance with Rule 47.1(c), third sentence, those Offices will accept the present Notice as conclusive evidence that the communication of the international application has duly taken place on the date of mailing indicated above and no copy of the international application is required to be furnished by the applicant to the designated Office(s).

2. The following designated Offices have waived the requirement for such a communication at this time:
   AE,AL,AM,AP,AT,AZ,BA,BB,BG,BR,BY,CA,CH,CU,CZ,DE,DK,EA,EE,ES,FI,GB,GD,GE,GH,GM,HR,HU,ID,IN,IS,KE,KG,KZ,LC,LK,LR,LS,LT,LU,LV,MD,MG,MK,MN,MW,MX,NO,NZ,OA,PL,PT,RO,RU,SD,SE,SG,SI,SK,SL,TJ,TM,TR,TT,UA,UG,UZ,VN,YU,ZA,ZW
   The communication will be made to those Offices only upon their request. Furthermore, those Offices do not require the applicant to furnish a copy of the international application (Rule 49.1(a-bis)).

3. Enclosed with this Notice is a copy of the international application as published by the International Bureau on
   23 September 1999 (23.09.99) under No. WO 99/48219

REMINDER REGARDING CHAPTER II (Article 31(2)(a) and Rule 54.2)

If the applicant wishes to postpone entry into the national phase until 30 months (or later in some Offices) from the priority date, **a demand for international preliminary examination** must be filed with the competent International Preliminary Examining Authority before the expiration of 19 months from the priority date.

It is the applicant's sole responsibility to monitor the 19-month time limit.

Note that only an applicant who is a national or resident of a PCT Contracting State which is bound by Chapter II has the right to file a demand for international preliminary examination.

REMINDER REGARDING ENTRY INTO THE NATIONAL PHASE (Article 22 or 39(1))

If the applicant wishes to proceed with the international application in the **national phase**, he must, within 20 months or 30 months, or later in some Offices, perform the acts referred to therein before each designated or elected Office.

For further important information on the time limits and acts to be performed for entering the national phase, see the Annex to Form PCT/IB/301 (Notification of Receipt of Record Copy) and Volume II of the PCT Applicant's Guide.

The International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland

Facsimile No. (41-22) 740.14.35

Authorized officer
J. Zahra

Telephone No. (41-22) 338.83.38

Continuation of Form PCT/IB/308

NOTICE INFORMING THE APPLICANT OF THE COMMUNICATION OF THE INTERNATIONAL APPLICATION TO THE DESIGNATED OFFICES

Date of mailing (day/month/year) 23 September 1999 (23.09.99)	IMPORTANT NOTICE
Applicant's or agent's file reference 4650/WO/98	International application No. PCT/IL99/00154

The applicant is hereby notified that, at the time of establishment of this Notice, the time limit under Rule 46.1 for making amendments under Article 19 has not yet expired and the International Bureau had received neither such amendments nor a declaration that the applicant does not wish to make amendments.

IPEA/ US

PCT

CHAPTER II

DEMAND

under Article 31 of the Patent Cooperation Treaty:
The undersigned requests that the international application specified below be the subject of international preliminary examination according to the Patent Cooperation Treaty.

For International Preliminary Examining Authority use only

Identification of IPEA	Date of receipt of DEMAND

Box No. I IDENTIFICATION OF THE INTERNATIONAL APPLICATION

Applicant's or agent's file reference: 4650/WO/98

International application No.	International filing date (day/month/year)	(Earliest) Priority date (day/month/year)
PCT/IL99/00154	18 March 1999 (18.03.99)	19 March 1998 (19.03.98)

Title of invention
METHOD AND APPARATUS FOR CLOCK TIMING RECOVERY IN XDSL, PARTICULARLY VDSL MODEMS

Box No. II APPLICANT(S)

Name and address:

SAVAN COMMUNICATIONS LTD.
71a Hamelacha Street
Netanya 42504
Israel

Telephone No.:

Facsimile No.:

Teleprinter No.:

State (i.e. country) of nationality: IL

State (i.e. country) of residence: IL

Name and address:

PORAT, Boaz
93 Shimshon Street
Haifa 34678
Israel

State (i.e. country) of nationality: IL

State (i.e. country) of residence: IL

Name and address:

HARPAK, Amnon
62 Moshe Dayan Street
Holon 58671
Israel

State (i.e. country) of nationality: IL

State (i.e. country) of residence: IL

☒ Further applicants are indicated on a continuation sheet.

International application No.
PCT/IL99/00154

Continuation of Box No. II APPLICANT(S)

If none of the following sub-boxes is used, this sheet is not to be included in the demand.

Name and address:

PELEG, Shimon
11 Anchilevich Street
Hod-Hasharon 45285
Israel

State (i.e. country) of nationality: IL	State (i.e. country) of residence: IL

Name and address:

State (i.e. country) of nationality:	State (i.e. country) of residence:

Name and address:

State (i.e. country) of nationality:	State (i.e. country) of residence:

Name and address:

State (i.e. country) of nationality:	State (i.e. country) of residence:

☐ Further applicants are indicated on another continuation sheet.

International application No.
PCT/IL99/00154

Box No. III AGENT OR COMMON REPRESENTATIVE; OR ADDRESS FOR CORRESPONDENCE

The following person is ☒ agent ☐ common representative

and ☒ has been appointed earlier and represents the applicant(s) also for international preliminary examination.

☐ is hereby appointed and any earlier appointment of (an) agent(s)/common representative is hereby revoked.

☐ is hereby appointed, specifically for the procedure before the International Preliminary Examining Authority, in addition to the agent(s)/common representative appointed earlier.

Name and address:

LUZZATTO, Kfir; LUZZATTO, Edgar; LUZZATTO, Esther; HACKMEY, Michal, FUERST, Zadok; PYERNIK, Moshe; MANZUROLA, Emanuel; SERUYA, Yehuda; PRICE, Eyal; SHALEV, Ronit; HACKMEY, Miriam
LUZZATTO & LUZZATTO
P.O.Box 5352
Beer-Sheva 84 152
Israel

Telephone No.: (972-7) 6497-871

Facsimile No.: (972-7) 6497-125

Teleprinter No.:

☐ Mark this check-box where no agent or common representative is/has been appointed and the space above is used instead to indicate a special address to which correspondence should be sent.

Box No. IV STATEMENT CONCERNING AMENDMENTS

The applicant wishes the International Preliminary Examining Authority*

(i) ☒ to start the international preliminary examination on the basis of the international application as originally filed.

(ii) ☐ to take into account the amendments under Article 34 of

☐ the description (amendments attached).

☐ the claims (amendments attached).

☐ the drawings (amendments attached).

(iii) ☐ to take into account any amendments of the claims under Article 19 filed with the International Bureau (a copy is attached).

(iv) ☐ to disregard any amendments of the claims made under Article 19 and to consider them as reversed.

(v) ☐ to postpone the start of the international preliminary examination until the expiration of 20 months from the priority date unless that Authority receives a copy of any amendments made under Article 19 or a notice from the applicant that he does not wish to make such amendments (Rule 69.1(d)).

* Where no check-box is marked, international preliminary examination will start on the basis of the international application as originally filed or, where a copy of amendments to the claims under Article 19 and/or amendments to the international application under Article 34 are received by the International Preliminary Examining Authority before it has begun to draw up a written opinion or the international preliminary examination report, as so amended.

Box No. V ELECTION OF STATES

☒ The applicant hereby elects all eligible States except .....

.....

.....

.....

International application No.
PCT/IL99/00154

Box No. VI CHECK LIST

The demand is accompanied by the following documents for the purposes of international preliminary examination:			For international Preliminary Examining Authority use only: received	not received
1. amendments under Article 34				
description	:	sheets	☐	☐
claims	:	sheets	☐	☐
drawings	:	sheets	☐	☐
2. letter accompanying amendments under Article 34	:	sheets	☐	☐
3. copy of amendments under Article 19	:	sheets	☐	☐
4. copy of statement under Article 19	:	sheets	☐	☐
5. other *(specify)*:	:	sheets	☐	☐

The demand is also accompanied by the item(s) marked below:

1. ☒ separate signed power of attorney
2. ☒ copy of general power of attorney
3. ☐ statement explaining lack of signature
4. ☒ fee calculation sheet
5. ☒ other *(specify)*: check

Box No. VII SIGNATURE OF APPLICANT, AGENT OR COMMON REPRESENTATIVE

Zadok Fuerst

For International Preliminary Examining Authority use only

1. Date of actual receipt of DEMAND:
2. Adjusted date of receipt of demand due to CORRECTIONS under Rule 60.1(b):
3. ☐ The date of receipt of the demand is AFTER the expiration of 19 months from the priority date and item 4 or 5, below, does not apply. ☐ The applicant has been informed accordingly.
4. ☐ The date of receipt of the demand is WITHIN the period of 19 months from the priority date as extended by virtue of Rule 80.5.
5. ☐ Although the date of receipt of the demand is after the expiration of 19 months from the priority date, the delay in arrival is EXCUSED pursuant to Rule 82.

For International Bureau use only

Demand received from IPEA on:

PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION OF THE RECORDING OF A CHANGE

(PCT Rule 92bis.1 and Administrative Instructions, Section 422)

To:

LUZZATTO, Kfir
Luzzatto & Luzzatto
P.O. Box 5352
84152 Beer-Sheva
ISRAËL

Date of mailing (day/month/year) 09 August 2000 (09.08.00)	
Applicant's or agent's file reference 4650/WO/98	**IMPORTANT NOTIFICATION**
International application No. PCT/IL99/00154	**International filing date** (day/month/year) 18 March 1999 (18.03.99)

1. The following indications appeared on record concerning:

[X] the applicant [ ] the inventor [ ] the agent [ ] the common representative

Name and Address	State of Nationality	State of Residence
SAVAN COMMUNICATIONS LTD. Hamelacha Street 71a 42504 Netanya Israel	IL	IL
	Telephone No.	
	Facsimile No.	
	Teleprinter No.	

2. The International Bureau hereby notifies the applicant that the following change has been recorded concerning:

[X] the person [X] the name [X] the address [ ] the nationality [ ] the residence

Name and Address	State of Nationality	State of Residence
INFINEON TECHNOLOGIES AG St. Martin Strasse 53 D-81541 Munich Germany	DE	DE
	Telephone No.	
	Facsimile No.	
	Teleprinter No.	

3. Further observations, if necessary:

4. A copy of this notification has been sent to:

[X] the receiving Office
[ ] the International Searching Authority
[ ] the International Preliminary Examining Authority
[ ] the designated Offices concerned
[X] the elected Offices concerned
[ ] other:

The International Bureau of WIPO **34, chemin des Colombettes** **1211 Geneva 20, Switzerland**	Authorized officer I. Britel
Facsimile No.: (41-22) 740.14.35	Telephone No.: (41-22) 338.83.38

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	**ES**	Spain	**LS**	Lesotho	**SI**	Slovenia
AM	Armenia	**FI**	Finland	**LT**	Lithuania	**SK**	Slovakia
AT	Austria	**FR**	France	**LU**	Luxembourg	**SN**	Senegal
AU	Australia	**GA**	Gabon	**LV**	Latvia	**SZ**	Swaziland
AZ	Azerbaijan	**GB**	United Kingdom	**MC**	Monaco	**TD**	Chad
BA	Bosnia and Herzegovina	**GE**	Georgia	**MD**	Republic of Moldova	**TG**	Togo
BB	Barbados	**GH**	Ghana	**MG**	Madagascar	**TJ**	Tajikistan
BE	Belgium	**GN**	Guinea	**MK**	The former Yugoslav Republic of Macedonia	**TM**	Turkmenistan
BF	Burkina Faso	**GR**	Greece			**TR**	Turkey
BG	Bulgaria	**HU**	Hungary	**ML**	Mali	**TT**	Trinidad and Tobago
BJ	Benin	**IE**	Ireland	**MN**	Mongolia	**UA**	Ukraine
BR	Brazil	**IL**	Israel	**MR**	Mauritania	**UG**	Uganda
BY	Belarus	**IS**	Iceland	**MW**	Malawi	**US**	United States of America
CA	Canada	**IT**	Italy	**MX**	Mexico	**UZ**	Uzbekistan
CF	Central African Republic	**JP**	Japan	**NE**	Niger	**VN**	Viet Nam
CG	Congo	**KE**	Kenya	**NL**	Netherlands	**YU**	Yugoslavia
CH	Switzerland	**KG**	Kyrgyzstan	**NO**	Norway	**ZW**	Zimbabwe
CI	Côte d'Ivoire	**KP**	Democratic People's Republic of Korea	**NZ**	New Zealand		
CM	Cameroon			**PL**	Poland		
CN	China	**KR**	Republic of Korea	**PT**	Portugal		
CU	Cuba	**KZ**	Kazakstan	**RO**	Romania		
CZ	Czech Republic	**LC**	Saint Lucia	**RU**	Russian Federation		
DE	Germany	**LI**	Liechtenstein	**SD**	Sudan		
DK	Denmark	**LK**	Sri Lanka	**SE**	Sweden		
EE	Estonia	**LR**	Liberia	**SG**	Singapore		

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IL99/00154

A. CLASSIFICATION OF SUBJECT MATTER
IPC(6) : H04B 1/38, 1/50; H04L 5/12, 5/16
US CL : 375/222, 261, 350
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 375/222, 223, 261, 350, 355; 379/93.09; 370/493, 494, 495

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS searched terms: ?dsl modem#

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5,163,044 A (GOLDEN) 10 November 1992, abstract, figures 3-4 and col. 2, lines 6-41.	1-14
A	US 5,222,077 A (KRISHNAN) 22 June 1993, abstract.	1-14
A	US 5,331,670 A (SORBARA et al) 19 July 1994, abstract and figure 6.	1-14

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 28 JUNE 1999	Date of mailing of the international search report 17 AUG 1999
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C 20231 Facsimile No. (703) 305-3230	Authorized officer DON N VO James R. Matthews Telephone No. (703) 305-4885

Form PCT/ISA/210 (second sheet)(July 1992)*

09/623952

16

5010

PATENT COOPERATION TREATY

RECD 31 JUL 2000

WIPO PCT

PCT

Corrected

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference 4650/WO/98	FOR FURTHER ACTION	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
International application No. PCT/IL99/00154	International filing date *(day/month/year)* 18 MARCH 1999	Priority date *(day/month/year)* 19 MARCH 1998
International Patent Classification (IPC) or national classification and IPC IPC(6): H04B 1/38, 1/50; H04L 5/12, 5/16 and US Cl.: 375/222, 261, 350		
Applicant SAVAN COMMUNICATIONS LTD.		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 4 sheets.

   ☒ This report is also accompanied by ANNEXES, i.e., sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority. (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 3 sheets.

3. This report contains indications relating to the following items:

   - I [X] Basis of the report
   - II [ ] Priority
   - III [ ] Non-establishment of report with regard to novelty, inventive step or industrial applicability
   - IV [ ] Lack of unity of invention
   - V [X] Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
   - VI [ ] Certain documents cited
   - VII [ ] Certain defects in the international application
   - VIII [X] Certain observations on the international application

Date of submission of the demand	Date of completion of this report
27 SEPTEMBER 1999	23 MAY 2000
Name and mailing address of the IPEA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer Carol Bidwell R DON N VO Telephone No. (703) 305-4885

Form PCT/IPEA/409 (cover sheet) (July 1998) ★

CORRECTED VERSION

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/IL99/00154

I. Basis of the report

1. With regard to the **elements** of the international application:*

☐ the international application as originally filed

☒ the description:
pages (See Attached) , as originally filed
pages _____ , filed with the demand
pages _____ , filed with the letter of _____

☒ the claims:
pages (See Attached) , as originally filed
pages _____, as amended (together with any statement) under Article 19
pages _____ , filed with the demand
pages _____ , filed with the letter of _____

☒ the drawings:
pages (See Attached) , as originally filed
pages _____ , filed with the demand
pages _____ , filed with the letter of _____

☒ the sequence listing part of the description:
pages (See Attached) , as originally filed
pages _____ , filed with the demand
pages _____ , filed with the letter of _____

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.
These elements were available or furnished to this Authority in the following language _____ which is:

☐ the language of a translation furnished for the purposes of international search (under Rule 23.1(b)).

☐ the language of publication of the international application (under Rule 48.3(b)).

☐ the language of the translation furnished for the purposes of international preliminary examination (under Rules 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

☐ contained in the international application in printed form.

☐ filed together with the international application in computer readable form.

☐ furnished subsequently to this Authority in written form.

☐ furnished subsequently to this Authority in computer readable form.

☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

☐ The statement that the information recorded in computer readable form is identical to the writen sequence listing has been furnished.

4. ☒ The amendments have resulted in the cancellation of:

☒ the description, pages NONE

☒ the claims, Nos. NONE

☒ the drawings, sheets/~~fig~~ NONE

5. ☒ This report has been drawn as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).**

** Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17).*

***Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.*

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. statement

Novelty (N)	Claims	1-14	YES
	Claims	NONE	NO
Inventive Step (IS)	Claims	1-14	YES
	Claims	NONE	NO
Industrial Applicability (IA)	Claims	1-14	YES
	Claims	NONE	NO

2. citations and explanations (Rule 70.7)

Claims 1-14 meet the criteria set out in PCT Article 33(2)-(4), because the prior art does not teach or fairly suggest, in combination, the arrangements of the data received at the slave modem as a sequence of symbols, is sampled at the symbol rate, converted to digital form, said sampled data been split to In-phase (I) and Quadrature (Q) channels, filtered with a digital Low-Pass Filter (LPF), sampled again at twice the symbol rate, and modulated each with the two discrete-time sequences in order to form a method for the fast, timing recovery of transmitted data between two XDSL modems as recited in claim 1 and variations of circuit arrangements as recited in claim 12 and further limitations of their respective dependent claims 2-11 and 13-14.

---------- NEW CITATIONS ----------

NONE

Supplemental Box
(To be used when the space in any of the preceding boxes is not sufficient)

Continuation of: Boxes I - VIII

I. BASIS OF REPORT:

This report has been drawn on the basis of the description,
page(s) 1-25, as originally filed.
page(s) NONE, filed with the demand.
and additional amendments:
NONE

This report has been drawn on the basis of the claims,
page(s) 26-29, as originally filed.
page(s) NONE, as amended under Article 19.
page(s) NONE, filed with the demand.
and additional amendments:
Pages 30-32, filed with the letter of 09 March 2000.

This report has been drawn on the basis of the drawings,
page(s) 1-6, as originally filed.
page(s) NONE, filed with the demand.
and additional amendments:
NONE

This report has been drawn on the basis of the sequence listing part of the description:
page(s) NONE, as originally filed.
pages(s) NONE, filed with the demand.
and additional amendments:
NONE

5. (Some) amendments are considered to go beyond the disclosure as filed:
NONE

(2) Subtracting the value of the DAC's LSB from the accumulator output, if the output value is smaller than half the value of the DAC's LSB.

11. A method according to any one of claims 1 to 10, substantially as described and illustrated.

12. An xDSL modem for fast timing recovery of received data, said data transmitted between two xDSL modems and transferred trough a noisy, high loss, high distortion wiring, comprising:

a) Circuitry for receiving the transmitted symbols at the slave receiver (demodulator);

b) Circuitry for sampling the received signal;

c) Circuitry for splitting the sampled data to in-phase (I) and quadrature (Q) channels;

d) Circuitry for filtering each channels of step c) above with digital low-pass filters, said filters being matched to the transmitting filters at the master modem;

e) Circuitry for turning the master clock timing recovery into blind mode, by the steps of:

(1) Circuitry for sampling the filtered I and Q outputs at twice the symbol rate;

(2) Circuitry for extracting the lower and upper band edge components by modulating each of the sampled sequence of I and Q outputs of step (1) above with two discrete time sequences: $\cos(0.5\pi n) = \ldots,1,0,-1,0,\ldots$; $\sin(0.5\pi n) = \ldots,0,1,0,-1,\ldots$

(3) Circuitry for filtering the four resulting products with four first order low-

pass filters and re-sampling the results at the symbol rate;

(4) Circuitry for computing the real and imaginary parts of the spectral line vector using the products of step (3) above;

(5) Circuitry for filtering both the real and the imaginary parts of step (4) above, using one or more first order low-pass filter;

(6) Circuitry for normalizing the magnitude of the spectral line vector to unity using a suitable automatic gain control circuitry;

(7) Circuitry for extracting the phase of the spectral line vector from the normalized imaginary part of step (6) above;

(8) Circuitry for feeding the sampled imaginary part of step (7) above as a phase-error signal to a controller of a phase-locked loop (PLL), said PLL utilizing a frequency controlled clock oscillator, the frequency of which is tuned to track the frequency of the incoming symbols (the master modem clock frequency);

(9) Circuitry for converting the digital control word to analog control voltage supplied to the tracking oscillator of step (8) above, using a Digital to Analog Converter (DAC);

f) Circuitry for feeding the I and Q filtered outputs to a complex linear equalizer for coarse phase and amplitude error correction;

g) Circuitry for computing the symbol state data decisions using a slicer circuitry;

h) Fine equalizing the channel distortions by feeding the I and Q outputs of the slicer to a decision feedback equalizer, the outputs of which is extracted from the slicer I and Q inputs, respectively;

i) Circuitry for computing the extracted symbols error rate at the slicer outputs; and

j) Circuitry for switching from blind mode timing recovery to data directed timing recovery mode, once the error is reduced to less than a given BER.

13. A modem according to claim 12, further comprising (10) circuitry for accumulation to correct the control word supplied to the DAC by providing:

a) Circuitry for rounding the double precision control signal;

b) Circuitry for generation of an error signal between the double precision value and the rounded value;

c) Circuitry for accumulation of the error signal in a secondary accumulator;

d) Circuitry for adding the error signal to the output signal of the secondary accumulator;

e) Circuitry for comparing the result of step (d) above with half the value of the DAC's LSB;

f) Circuitry for compensating the rounded value according to the result of step (e) above and by:

(1) Circuitry for adding the value of the DAC's LSB to the accumulator output, if the output value is larger than half the value of the DAC's LSB; and

(2) Circuitry for subtracting the value of the DAC's LSB from the accumulator output, if the output value is smaller than half the value of the DAC's LSB.

14. A modem according to claim 12, comprising means for sampling at a sampling rate that is more than twice the symbol rate.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1-14 (canceled)

What is claimed is:

15. (new) A method for fast clock timing recovery ~~from transmitted~~ of data between a master XDSL modem and a slave XDSL modem wherein said data is submitted over an XDSL transmission medium comprising the steps of:

why capital?

(a) Providing the master XDSL modem, synchronized by its own timing clock, for data transmission,

(b) Providing the slave XDSL modem, synchronized by its own timing clock, for data reception,

(c) Providing the transmission medium connecting the master and the slave XDSL modems,

(d) Encoding and transmitting the data at the ~~mater~~ master XDSL modem as a sequence of symbols using pre-determined QAM states, said sequence having a frequency,

(e) Receiving the data at the slave XDSL modem as said sequence of symbols,

(f) Sampling the received data at a symbol rate and converting the sampled data into a digital form,

(g) Splitting the digitally converted data into in-phase (I) and quadrature (Q) channels,

(h) Low-pass filtering of the digitally converted data corresponding to the in-phase and quadrature channels,

(i1) Re-sampling the filtered data at a re-sampling rate which is at least twice the symbol rate,

(i2) Modulating each of said re-sampled data with the two discrete-time sequences:

$\cos(0.5\,\pi\,n) = \ldots, 1, 0, -1, 0, \ldots$

$\sin(0.5\,\pi\,n) = \ldots, 0, 1, 0, -1, \ldots$

(i3) Computing a normalized spectral line vector corresponding to the re-sampled modulated data,

(i4) Tuning the symbol rate in dependence of the imaginary part of the normalized spectral line vector for tracking the frequency of the incoming symbols, for fast clock-timing recovery.

16. (new) The method according to claim 15 wherein the step h) of low-pass filtering comprises filtering each channel with digital low-pass filters, said filters being matched to transmitting filters at the master XDSL modem; and the steps i1) to i4) comprise turning the clock timing recovery into a blind mode, by the steps of:

(a) Re-sampling the filtered I and Q data at twice the symbol rate;

(b) Extracting lower and upper band edge components by modulating each of the sampled sequence of I and Q data of step (a) above with the said two discrete time sequences;

(c) Filtering the four resulting products with four first order low-pass filters and re-sampling the results at the symbol rate;

(d) Computing real and imaginary parts of the corresponding normalized spectral line vector using the products of step (c) above;

(e) Filtering both the real and the imaginary parts of step (4) above, using another first order low-pass filter;

(f) Normalizing the magnitude of the spectral line vector to unity using a suitable automatic gain control circuitry;

(g) Extracting the phase of the spectral line vector from the normalized imaginary part of step (6) above;

(h) Feeding the imaginary part of step (7) above as a phase-error signal to a controller of a phase-locked loop (PLL), said controller outputting a digital control signal, said PLL utilizing a frequency controlled clock tracking oscillator, the frequency of which is tuned to track the frequency of the received sequence of symbols (the master modem clock frequency);

(i) Converting the digital control signal to an analog control voltage supplied to the clock tracking oscillator of step (8) above, using a Digital to Analog Converter (DAC); and

(j) Using a secondary accumulator to correct the control word supplied to the DAC of step (9) above.

17. (new) The method according to claim 16 wherein the method further comprises the steps:

(a) Feeding the filtered I and Q data to a complex linear equalizer for coarse phase and amplitude error correction;

(b) Computing symbol state data decisions and outputting said decisions using a slicer circuitry;

(c) Fine equalization of channel distortions by feeding the I and Q outputs of the slicer to a decision feedback equalizer, the outputs of which are extracted from the slicer ~~I and Q inputs, respectively~~;

(d) Computing an extracted symbols error rate at the slicer outputs; and

(e) After an error probability decreases to a given BER, switching from blind mode timing recovery to a data directed timing recovery mode.

18. (new) The method according to claim 15 wherein the transmission medium is a pair of copper wires.

19. (new) The method according to claim 15 wherein the ~~pair of~~ copper wires ~~is a~~ are telephone line.

20. (new) The method according to claims 16 wherein the tracking oscillator utilized by the ~~phase-locked loop~~ is a Voltage-Controlled Crystal Oscillator (VCXO).

21. (new) The method according to claim 16 wherein the blind timing recovery is achieved using a reduced constellation.

22. (new) The method according to claim 21 wherein the reduced constellation comprises only equal amplitude symbols.

23. (new) The method according to claim 16 wherein the blind timing recovery is achieved using full constellation.

24. (new) The method according to claim 16 wherein the digital control signal of the PLL tracking oscillator is provided accurately in double precision and converted using an up to 8 bit ~~Digital-to-Analog Converter (DAC) means~~, the method further comprising the steps of:

(a) Rounding the double precision control signal;

(b) Generating an error signal between the double precision value and the rounded value;

(c) Accumulating the error signal in a secondary accumulator;

(d) Adding the error signal to the output signal of the secondary accumulator;

(e) Comparing the result of step d) above with half the value of the DAC's LSB;

(f) Compensating the rounded value according to the result of step e) above by the steps of:

(g) Adding the value of the DAC's LSB to the secondary accumulator output, if the result output-value is larger than half the value of the DAC's LSB; or

(h) Subtracting the value of the DAC's LSB from the secondary accumulator output, if the result output-value is smaller than half the value of the DAC's LSB.

25. (new) An XDSL modem for fast clock timing recovery from a received data signal, said data signal is transmitted by a master XDSL modem and transferred over an XDLS-transmission medium, comprising:

(a) An input for receiving the transmitted data signal comprising a sequence of symbols, said sequence having a frequency;

(b) A first Analog to Digital Converter connected to the input for sampling and digitizing the received data signal at a symbol rate;

(c) Two first multipliers connected to the first Analog to Digital Converter for splitting the sampled and digitized data signal into in-phase (I) and quadrature (Q) channels, one of said two first multipliers being phase-shifted by 90°;

(d) Two first digital low-pass filters for filtering each channel, said filters being connected to the two first multipliers and being matched to transmitting filters at the XDSL master modem;

(e) A clock timing recovery circuit operating in blind mode, comprising:

(1) Means for sampling the filtered I and Q channels at twice the symbol rate;

(2) Four second multipliers connected to the sampling means ~~for sampling~~ for modulating each of the sampled sequence of I and Q channels with two discrete time sequences:

$\cos(0.5\,\pi\,n) = \ldots, 1, 0, -1, 0, \ldots$

$\sin(0.5\,\pi\,n) = \ldots, 0, 1, 0, -1, \ldots$

for extracting lower and upper band edge components;

21~24 (3) Four second first order low-pass filters connected to the four second multipliers for filtering the four resulting products of the four second multipliers and for resampling the results at the symbol rate;

25 (4) A spectral line computer connected to the four second first order low-pass filters for computing real and imaginary parts of a spectral line vector;

26, 27 (5) At least one third first order low-pass filter connected to the spectral line computer for filtering both the real and the imaginary parts of the spectral line vector;

28 (6) A spectral line normalizer connected to the at least one third first order low-pass filters for normalizing the magnitude of the spectral line vector to unity using a suitable automatic gain control circuitry;

29 (7) A Controller connected to the spectral line normalizer, the controller being part of a phase-locked loop (PLL) and said controller outputting a digital control signal, said PLL utilizing a frequency controlled clock tracking oscillator, the frequency of which is tuned to track the frequency of the received sequence of symbols (or the master modem clock frequency);

(8) A second Digital to Analog Converter (DAC) connected to the controller for converting the digital control signal to an analog control voltage supplied to the tracking oscillator of the PLL:

(f) A complex linear equalizer connected to the two first multipliers for coarse phase and amplitude error correction;

(g) A slicer circuitry connected to the complex linear equalizer for computing and outputting I and Q symbol state date decisions;

(h) A decision feedback equalizer connected to the outputs of the slicer circuitry and connected via an adder to the slicer circuitry input for fine equalizing channel distortions;

(i) Circuitry connected to the outputs of the slicer circuitry for computing an extracted symbols error rate; and

(j) Circuitry for switching from blind timing recovery mode to data directed timing recovery mode, once the error is reduced to less than a given BER.

26. (new) The modem according to claim 25 wherein the modem further comprises:

(9) A circuitry for accumulation to correct the digital control signal supplied to the second DAC, said digital control signal having double precision accuracy, comprising:

(a) Circuitry for rounding the double precision digital control signal;

(b) Circuitry for generation of an error signal between the double precision value and the rounded value;

(c) Circuitry for accumulation of the error signal in a secondary accumulator;

(d) A first adder for adding the error signal to the output signal of the secondary accumulator;

(e) A comparator for comparing the output of the adder with half the value of the second DAC's LSB;

(f) A second adder for compensating the rounded value according to the result of the comparator by

(i1) Adding the value of the second DAC's LSB to the accumulator output, if the output value is larger than half the value of the second DAC's LSB, and

(i2) Subtracting the value of the second DAC's LSB from the accumulator output, if the output value is smaller than half the value of the second DAC's LSB.